A New Family of High-Performance Parallel Decimal Multipliers*

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Outline

- Introduction. Previous work.
- Implementation of decimal parallel multiplication:
  - Fast carry-save addition using non conventional BCD.
  - Design of high-performance decimal *p:2* CSAs.
  - Parallel partial product generation.
- Architectures.
  - Signed-digit (SD) Radix-10.
  - SD Radix-4/Radix-5 (combined binary/decimal).
- Evaluation and Comparison.
- Conclusions.

Introduction

- High-performance decimal floating-point units.
- Parallel multiplier: scaling performance by pipelining.
- Multiplication stages:
  1. Generation of partial products (PPG)
  2. Reduction of partial products (PPR)
  3. Conversion to non-redundant representation.

- Problems of decimal implementation:
  - High value-range for decimal digits (0-9) → PPG
  - Inefficiency of conventional BCD coding → PPG, PPR

Previous Work on Decimal Multiplication

- Previous proposals for PPG
  1. Direct generation of partial products (digit-by-digit)
  2. Using multiplicand multiples (X,2X,3X,4X,…,9X).
     - Direct implementation.
     - SD multiplier. [Ex. 2 radix5 digits (-5X, 5X) (-2X,-X, X,2X)]
- Previous proposals for PPR
  1. Carry-save BCD-8421.
     a. Full BCD operands (3:2 CSAs + correction)
     b. Carry operand 1 bit each 4-bit. (4-bit decimal CPAs)
  2. Signed-digit representation for decimal digits.
     - SD adders more complex than CSA based implementations.

Proposed techniques

- X multiplicand, Y multiplier → BCD integer words.
- BCD digit represented as:

$$Z_i = \sum_{j=0}^{3} z_{i,j} r_j$$

BCD-8421 ($r_j=2^j$)
BCD-4221 (r_3,r_2,r_1,r_0) = (4,2,2,1)
BCD-5211 (r_3,r_2,r_1,r_0) = (5,2,1,1)

1. Decimal carry-save addition using BCD-4221.
2. Implementation of decimal CSAs for PPR.
3. Implementation of PPG using multiplier recoding:
   - SD radix-10
   - SD radix-4.
   - SD radix-5.

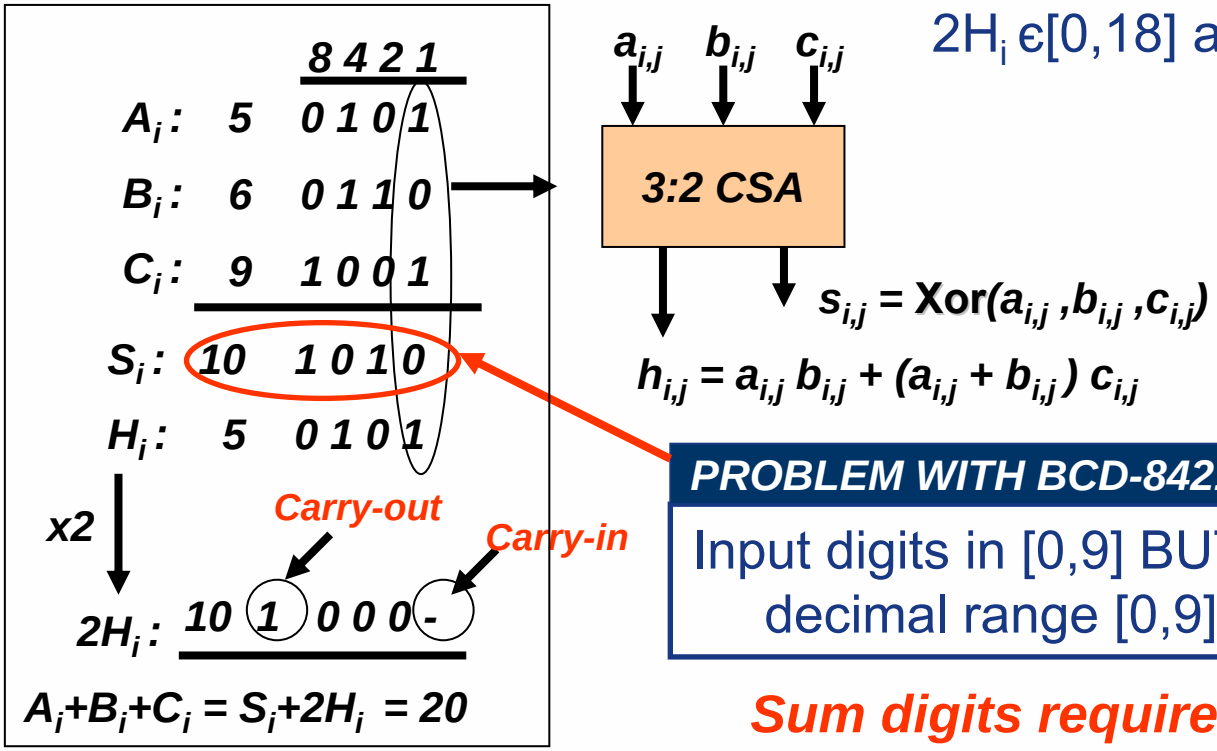
Decimal carry-save addition (BCD-8421)

- Add 3 decimal digits to produce 2 decimal digits (sum and carry digits).

$A_i+B_i+C_i = S_i+2H_i$

$A_i,B_i,C_i,S_i,H_i \in [0,9]$

$2H_i \in [0,18]$ and even



PROBLEM WITH BCD-8421

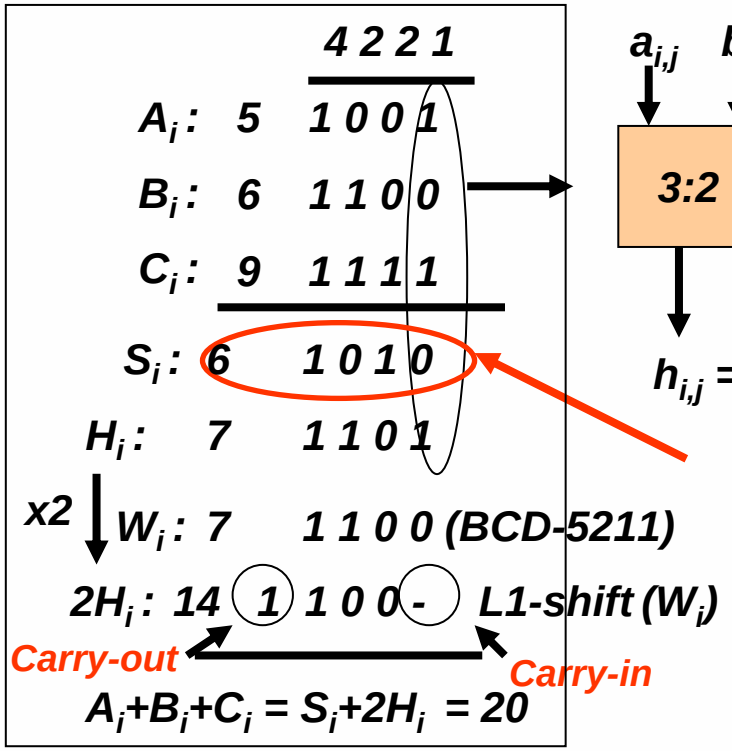
Input digits in [0,9] BUT *Sum digit* out of decimal range [0,9] ->[0,16]

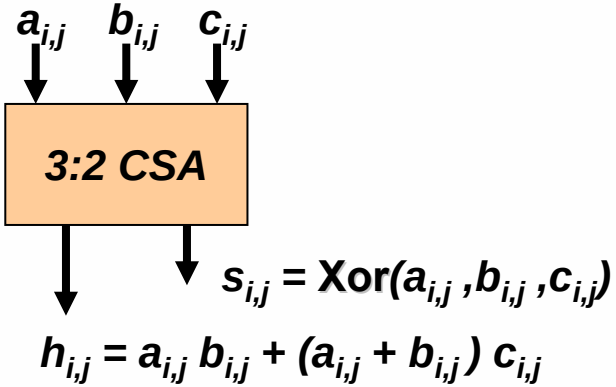
Sum digits require correction

Decimal carry-save addition (BCD-4221)

- Add 3 decimal digits to produce 2 decimal digits (sum and carry digits).

$A_i+B_i+C_i = S_i+2H_i = S_i+$***L1-shift***$(W_i)$ $A_i,B_i,C_i,S_i,H_i,W_i \in [0,9]$





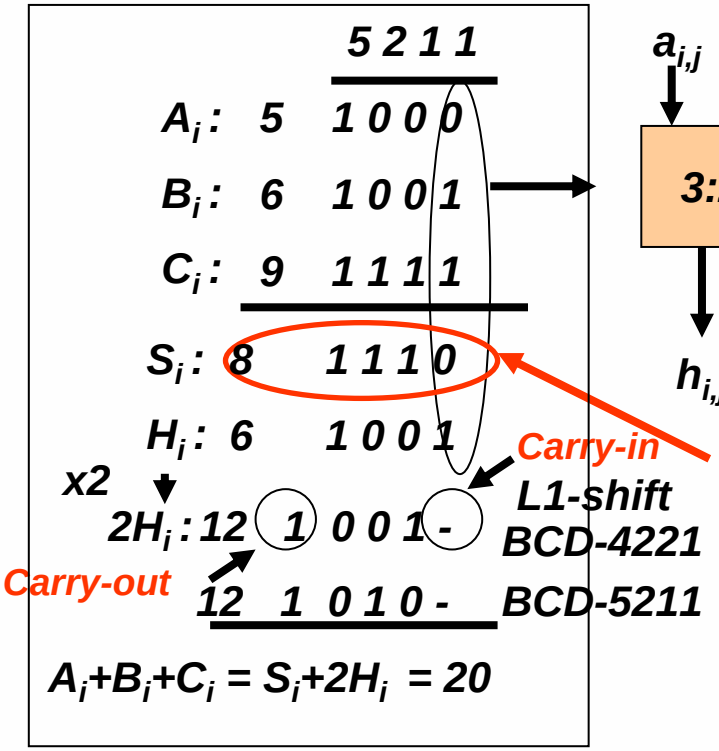
SOLUTION WITH BCD-4221

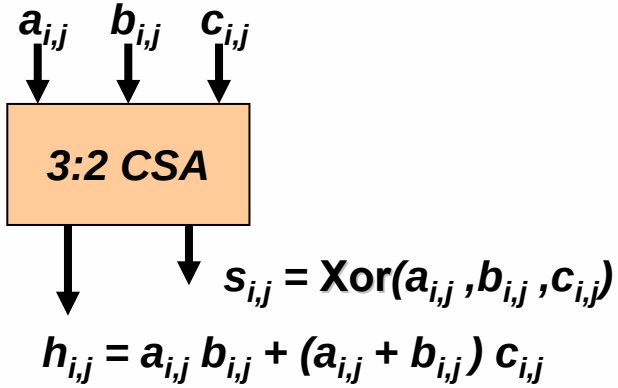
Input digits in [0,9] and *Sum digit* always in range [0,9].

Decimal carry-save addition (BCD-5211)

- Add 3 decimal digits to produce 2 decimal digits (sum and carry digits).

$A_i+B_i+C_i = S_i+2H_i = S_i+\textbf{\textit{L1-shift}}(H_i)_{BCD\text{-}4221}$ $\quad A_i,B_i,C_i,S_i,H_i \in [0,9]$



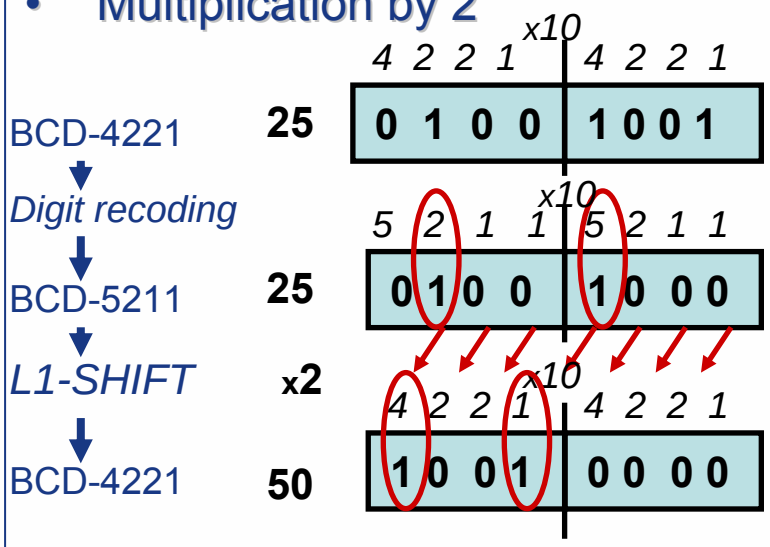


SOLUTION WITH BCD-5211

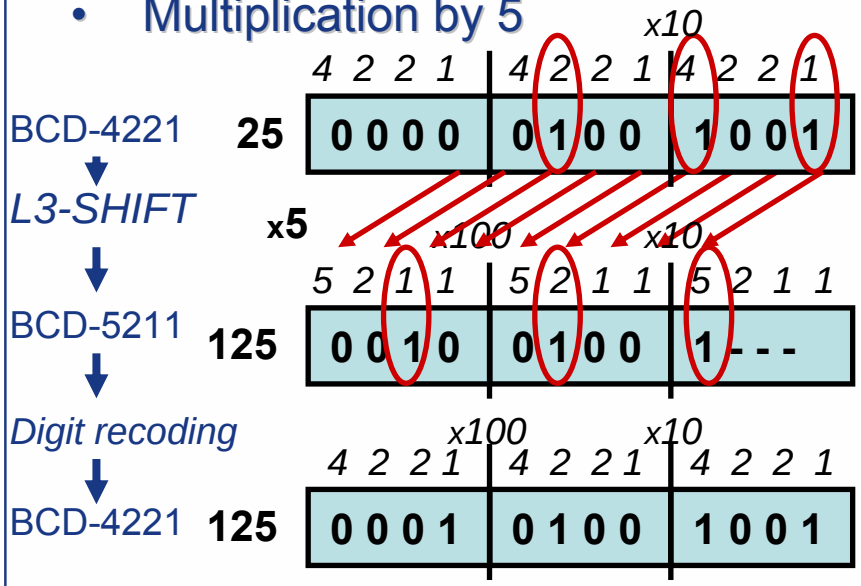
Input digits in [0,9] and *Sum digit* always in range [0,9].

Decimal multiplication by $\pm 2^n$ and $\pm 5^n$

- Multiplication by 2



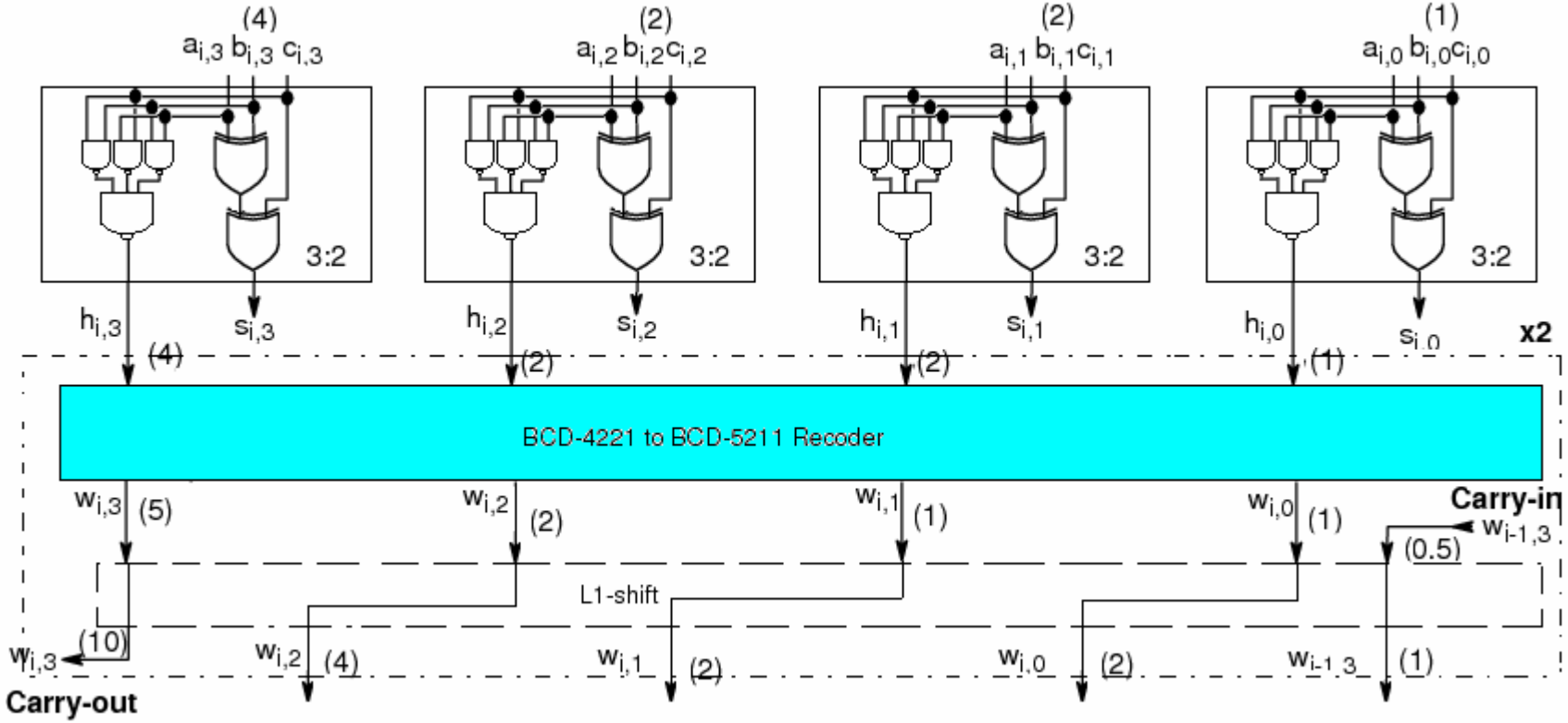
- Multiplication by 5



- Negative operands (10's complement) by bit inversion (2's complement)

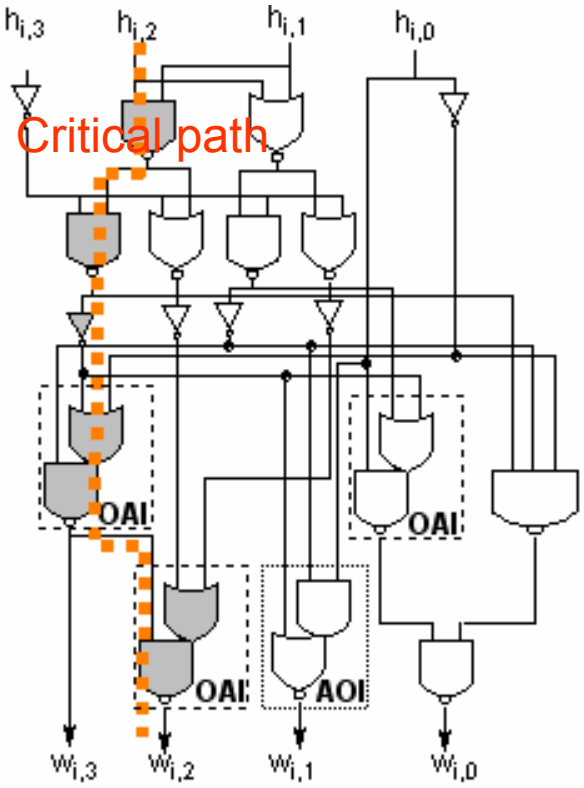
Proposed decimal 3:2 CSA (BCD-4221)

$$A_i+B_i+C_i = S_i+2H_i = S_i+\textbf{\textit{L1-shift}}(W_i)$$



Proposed decimal 3:2 CSA (BCD-4221)

	BCD-4221	BCD-5211
0	0000	0000
1	0001	0001
2	0010 0100	0100
3	0011 0101	0101
4	0100 0110	0111
5	1001 0111	1000
6	1100 1010	1010
7	1101 1011	1011
8	1110	1110
9	1111	1111



Digit recoder

BCD-4221 to BCD-5211

AREA: 18 NAND2

(0.35 times 4-bit 3:2 CSA area)

DELAY: 4 FO4

(0.9 times binary 3:2 CSA delay)

Decimal (digit) 3:2 CSA

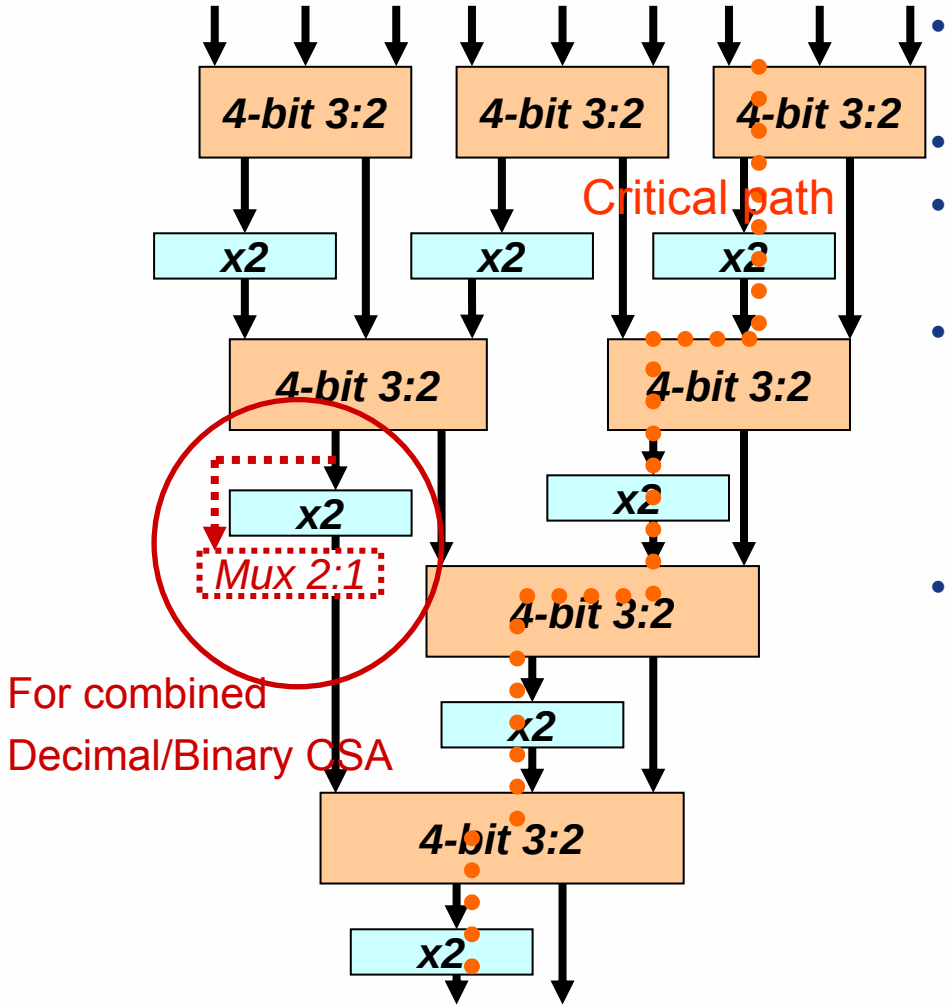
AREA: 66 NAND2

(1.35 times 4-bit 3:2 CSA area)

***DELAY: 1.4** times carry path/**same** sum path

*Ratio respect sum path (critical path) delay of bin. 3:2 CSA.

Decimal CSA tree (BCD-4221)

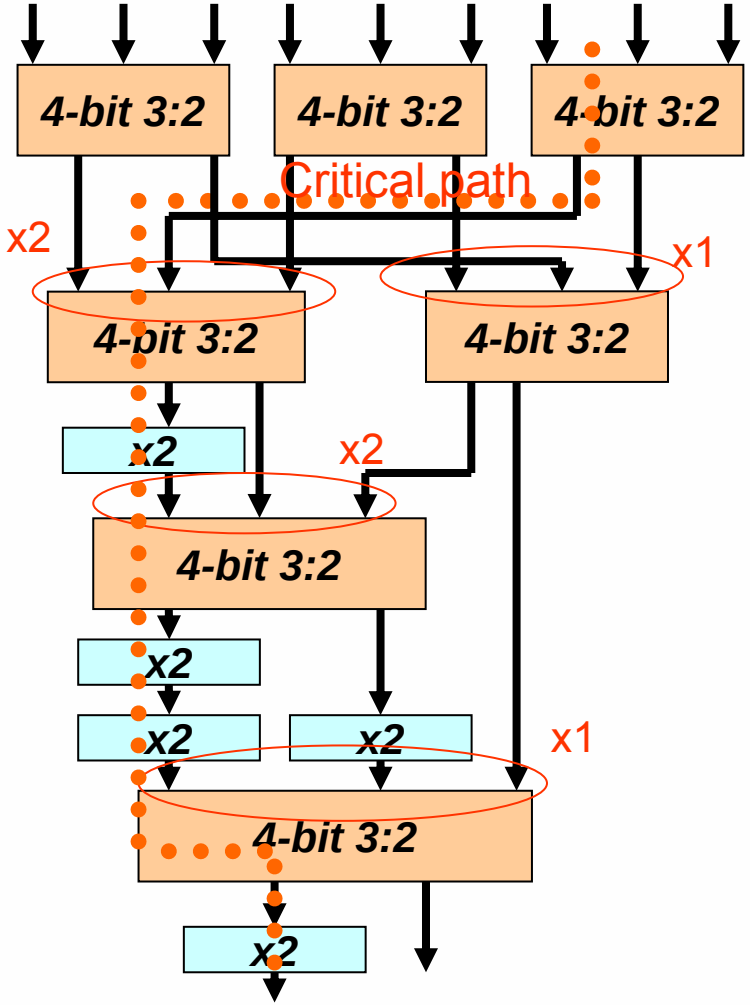


- **Example:** 9:2 Decimal CSA (digit slice).
- **1.35 area ratio** resp. binary CSA.
- **1.40 delay ratio** resp. binary CSA.

- Hardware complexity (1 digit):
  - 4-bit 3to2: 7x48 NAND2
  - Digit recoder (x2): 7x18 NAND2.

- Critical path delay:
  - 1-bit 3to2: 4.5/2.2 FO4 (2/1 XOR)
  - Recoder: 4 FO4 (1.75 XOR)
  - 9:2 Decimal CSA: 25 FO4.
  - 9:2 Binary CSA: 18 FO4.

Decimal CSA tree BCD-4221 (area-optimized)



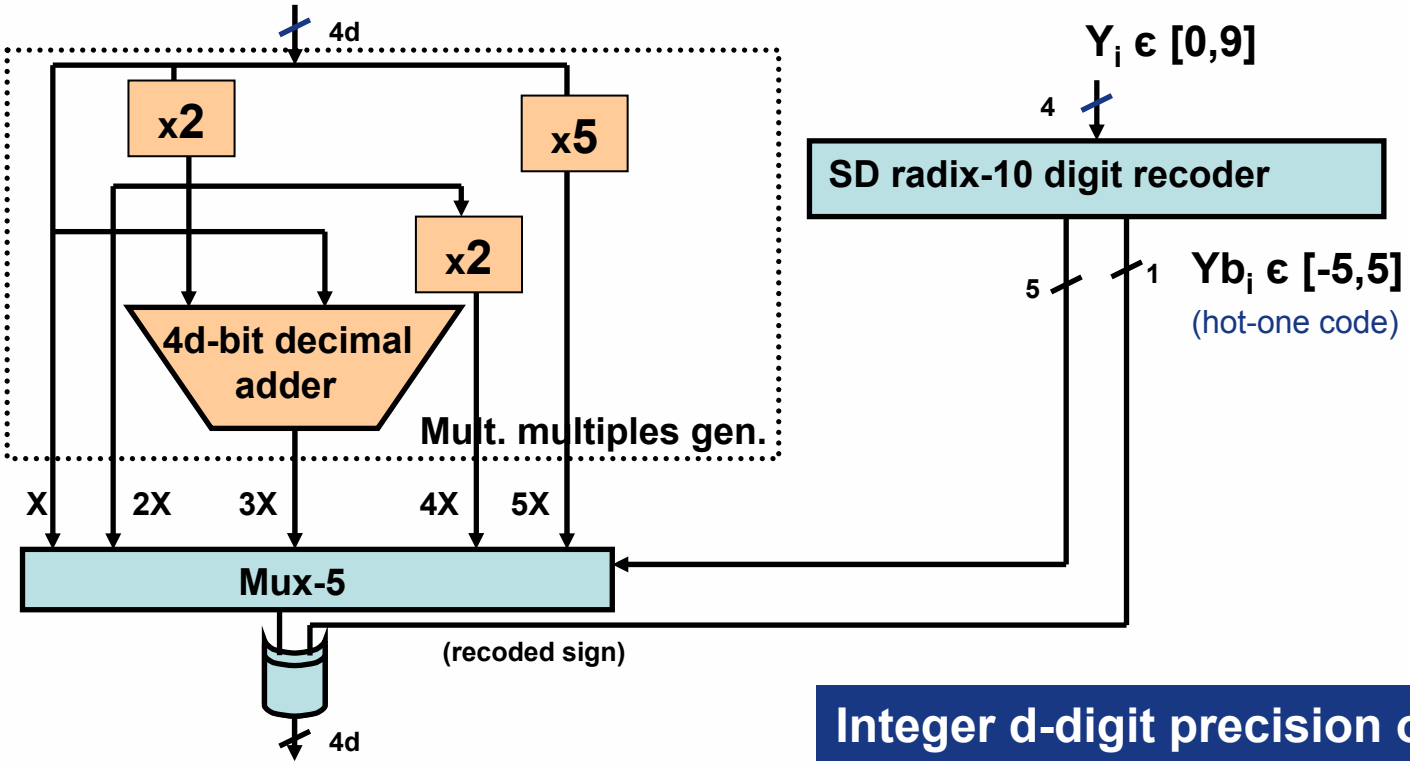
- **Example:** 9:2 Decimal CSA (digit slice).
- **Area optimization**: Group inputs with similar multiplicative factor.
- **1.20 area ratio** resp. binary CSA.
- **1.40 delay ratio** resp. binary CSA.

- Hardware complexity (1 digit):
  - 4-bit 3to2: 7x48 NAND2
  - Digit recoder (x2): 5x18 NAND2.

- Critical path delay:
  - 9:2 Decimal CSA: 25 FO4.
  - 9:2 Binary CSA: 18 FO4.

SD radix-10 multiplier recoding

- Multiplicand **X** (BCD-4221)
- Multiplier **Y** (BCD-8421)

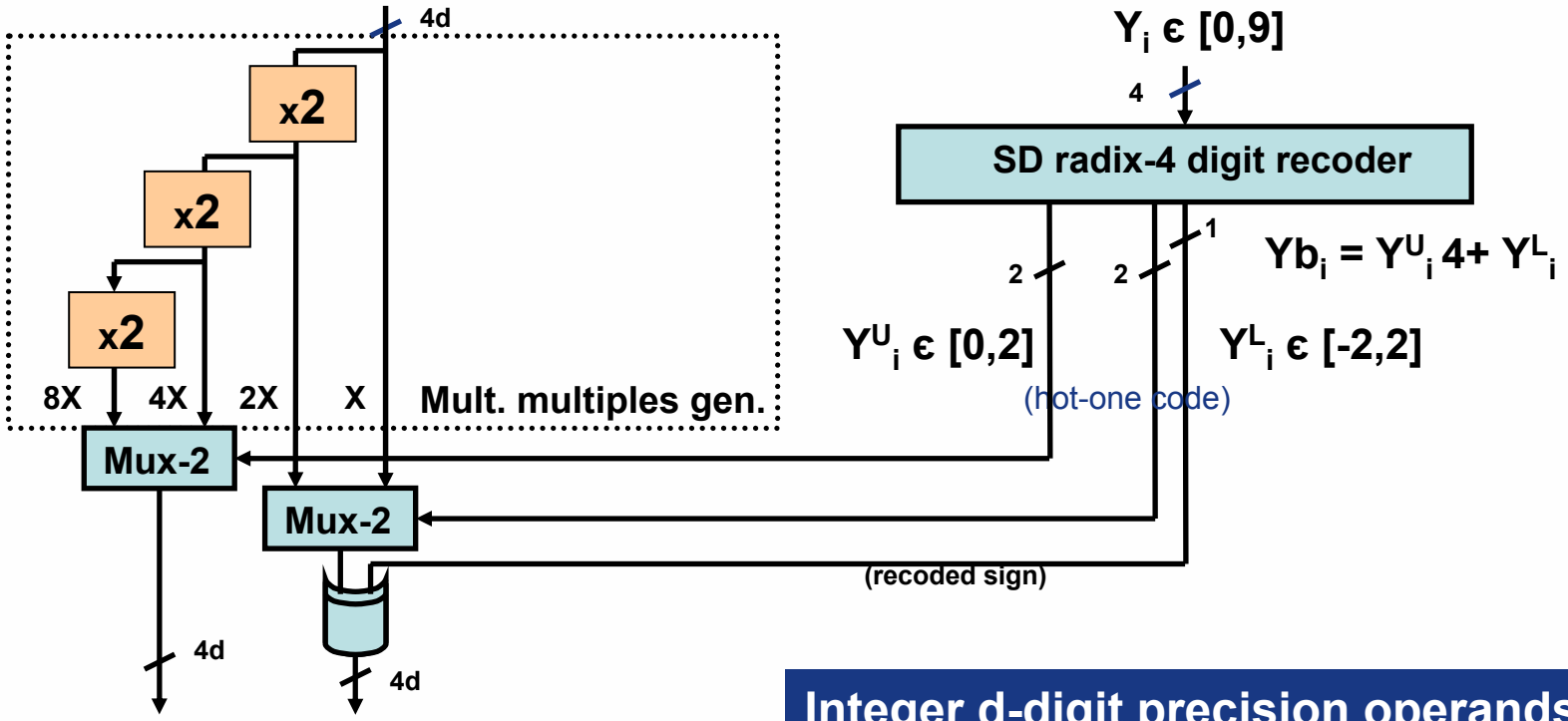


Integer d-digit precision operands

- **1 SD radix-10 digit/multiplicand digit**
- **d+1 partial products (additional encoded SD radix-10 digit)**

SD radix-4 multiplier recoding

- Multiplicand **X** (BCD-4221)
- Multiplier **Y** (BCD-8421)

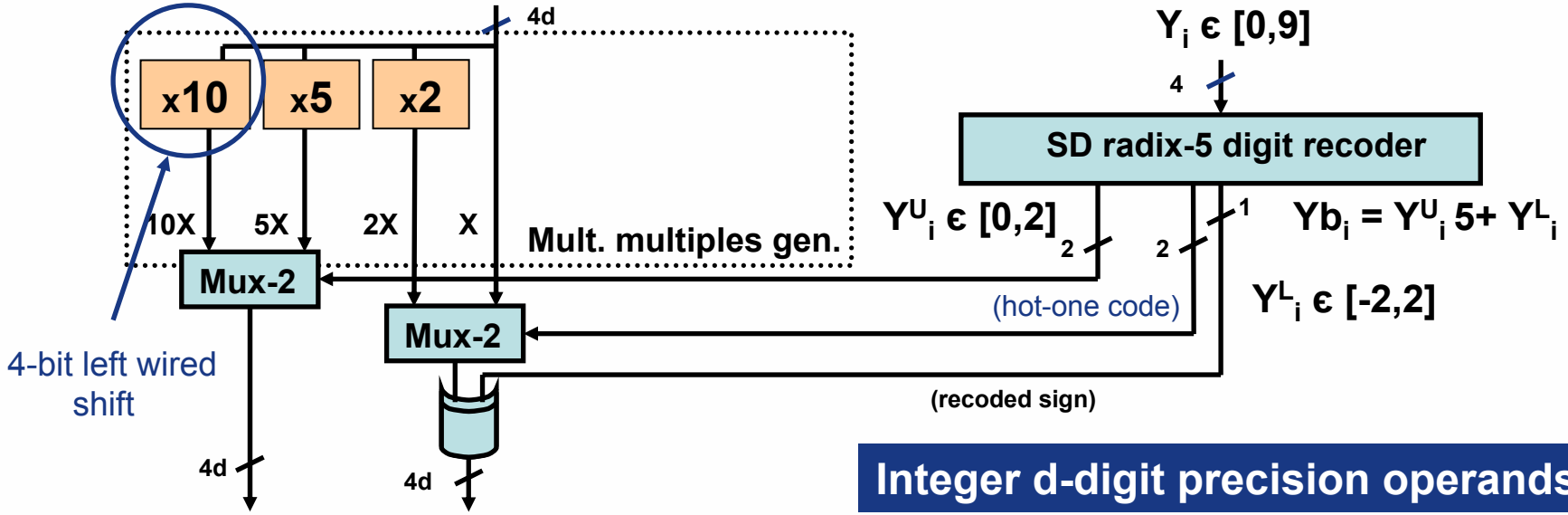


Integer d-digit precision operands

- **2 SD radix-4 digit/multiplicand digit**
- **2d partial products**

SD radix-5 multiplier recoding

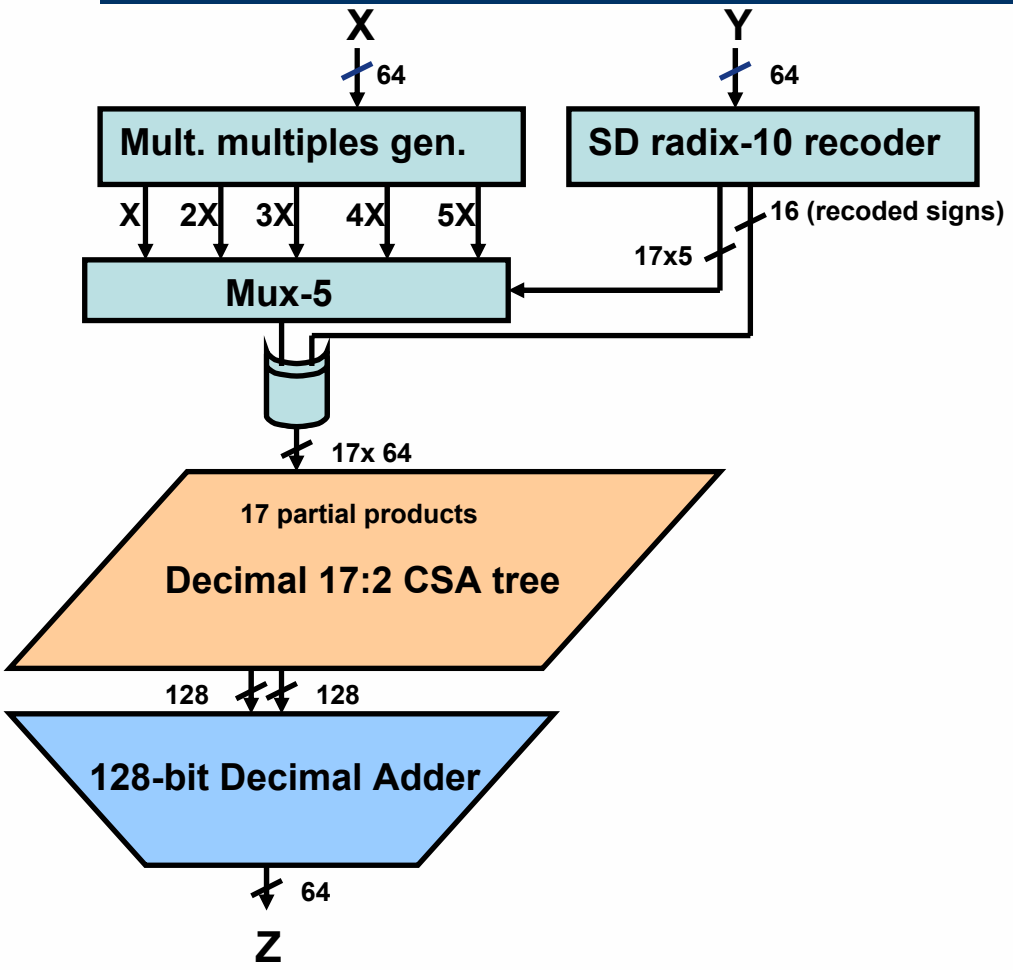
- Multiplicand **X** (BCD-4221)
- Multiplier **Y** (BCD-8421)



Integer d-digit precision operands

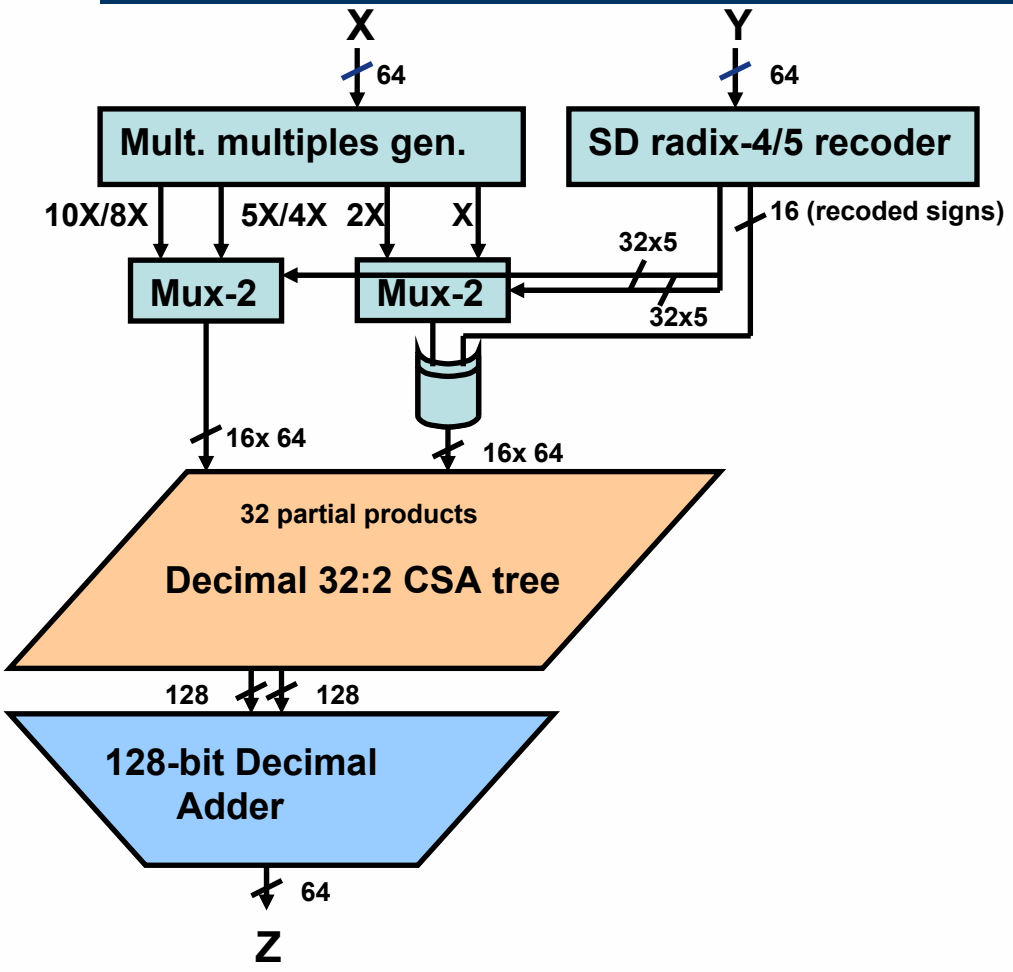
- **2 SD radix-5 digit/multiplicand digit.**
- **2d partial products**
- **Simple PPG: area/latency figures similar as Booth radix-4.**

Radix-10 architecture



- **Z= X x Y** only decimal multiplications.
- 16 BCD-digit (64 bits) significands (IEEE-754r Decimal64 format).
- **SD radix-10** multiplier recoding.
- 17 partial products generated.
- **Easily pipelined.**

Radix-4/5 architecture



- Can perform binary/decimal multiplications **Z= X x Y**.
- **SD radix-5/4** multiplier recoding (2 SD digits/BCD digit)
- **32 partial products** generated.
- **Easily pipelined.**

Evaluation results

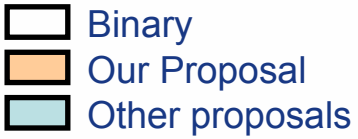
- Area-delay model based on logical effort (delay in FO4;area in NAND2)

Architecture (64-bits)	Delay (FO4)	Ratio	Area (Nand2)	Ratio
Bin. radix-4	50	1.0	43000	1.0
Bin. radix-8	57	1.15	39500	0.90
Dec. radix-4	70	1.4	49500	1.15
Dec. radix-5	65	1.3	49000	1.10
Bin/dec. radix-4	59/75	1.2/1.5	54000	1.25
Bin/dec. radix-4/5	61/71	1.2/1.4	53500	1.25
Dec. Radix-10	72	1.45	40000	0.90
Proposed in [8]	92	1.85	69000	1.60

[8] T. Lang and A. Nannarelli. *A radix-10 combinational multiplier*. Proc. 40th Asilomar Conf. on Signals, Systems, and Computers, pp 313–317, Oct. 2006.

Comparison of decimal carry-free trees

Architecture carry-free adder	Delay Ratio	Area Ratio
Binary 16:2 CSA	0.70	0.85
Decimal 16:2 CSA (area optimized)	1.00	1.00
SD tree [5,14]	2.00	2.90
4-bit CLA tree [4,7]	1.45	1.40
BCD-8421 CSA [11]	1.50	2.60
Non Spec. CSA [6]	1.30	1.45



[4] M. A. Erle and M. J. Schulte. *Decimal multiplication via carry-save addition*. In Proc. IEEE Int'l Conference on Application-Specific Systems, Architectures, and Processors, pp. 348–358, June 2003.

[5] M. A. Erle, E. M. Schwarz, and M. J. Schulte. *Decimal multiplication with efficient partial product generation*. Proc. IEEE 17th Symposium on Computer Arithmetic, pp. 21–28, June 2005.

[6] R. D. Kenney and M. J. Schulte. *High-speed multioperand decimal adders*. IEEE Trans. on Computers, 54(8):953–963, Aug. 2005.

[7] R. D. Kenney, M. J. Schulte, and M. A. Erle. *High-frequency decimal multiplier.* In Proc. IEEE Int'l Conference on ComputerDesign: VLSI in Computers and Processors, pp. 26–29, Oct. 2004.

[11] T. Ohtsuki. *Apparatus for decimal multiplication*. U.S.Patent No. 4,677,583, June 1987.

[14] B. Shirazi, D. Y. Y. Yun, and C. N. Zhang. *RBCD: Redundant binary coded decimal adder*. IEE Proc - Computers and Digital Techniques, 136(2):156–160, Mar. 1989.

Conclusions

- New family of parallel decimal multipliers: decimal radix-10 and combined radix-4/5 architectures.
- **Decimal carry-save addition** algorithm using **BCD-4221** (also valid for BCD-5211).
- Efficient designs of **decimal *p:2* CSA trees** for PPR.
- Parallel PPG using multiplicand multiples and three different SD recodings of the multiplier.
- **Area-delay figures outstand** other proposals and **comparable** to **binary parallel multipliers** (1.3/1.1 latency/area ratios for decimal SD radix-5 resp. binary Booth radix-4).
- **Future work**: decimal floating-point VLSI implementations.