Serial Parallel Multiplier Design in Quantum-dot Cellular Automata

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Outline

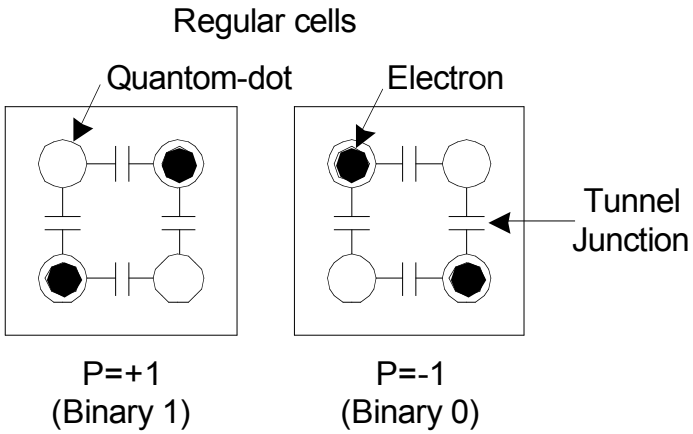
- Motivation
- Quantum-dot Cellular Automata
- Serial Multiplier Designs in QCA
- Conclusions

Quantum-dot Cellular Automata (QCA)

- Alternative to Transistor Technologies
  - Avoids High Power Consumption Due to Leakage Currents
- Quantum-dot Cellular Automata (QCA)
  - Emerging Nanotechnology for Electronic Circuits
    - Introduced in 1993
    - Freedom from Complicated Physics
  - High Density, Low Power Consumption, and Fast
  - Some Experimental Devices Have Been Created
- Several QCA Circuits Have Been Proposed
  - Ripple Carry Adders, Barrel Shifters, and Memories
  - Complex Designs Rare
- Key Characteristics
  - Inverters and 3-Input Majority Gates
  - Interconnect Consumes Time and Space
    - Difficult to Estimate Timing Until the Layout is Done
  - Signal Synchronization and Refresh
    - Wires Act as Latches
    - Best for Pipeline Architectures Without Feedback

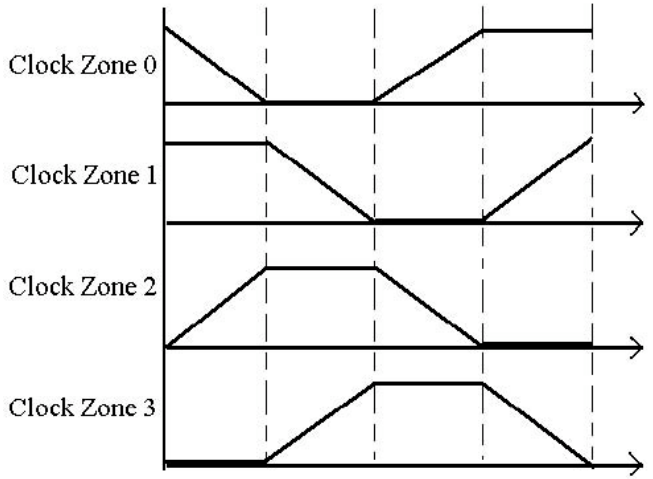
Basic Quantum-dot Cell

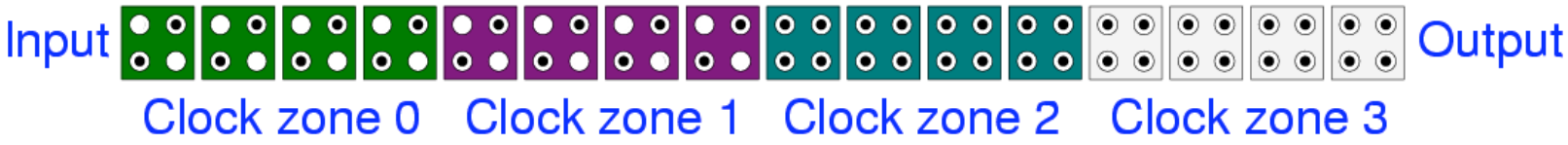
- Square Nanostructure
  - Each Cell
    - Has Four Quantum Dots
    - Can Possess a Single Electron per Dot
    - Charged With Two Electrons
  - Two Polarizations are Possible by Coulombic Repulsion



Signal Propagation

- Main Roles of Cells
  - Computation, Storage, and Communication
  - Wire Dominant Design
- Series of QCA Cells
  - Act Like a Wire
  - Propagate the Signal
- Clock Zones
  - Four Clock Phases
  - Control the Signal Flow
  - Cells Are Refreshed on Every Cycle

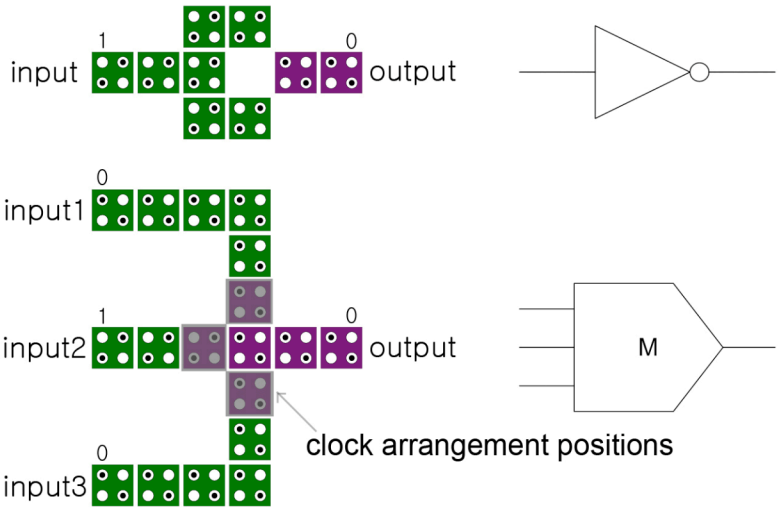




Fundamental Gates

- Inverter
  - Conventional Gate
- 3-Input Majority Gate

$$M(a,b,c) = a \cdot b + b \cdot c + c \cdot a$$



- 2-Input AND/OR Gate
  - Implemented by Setting One Input to a Constant

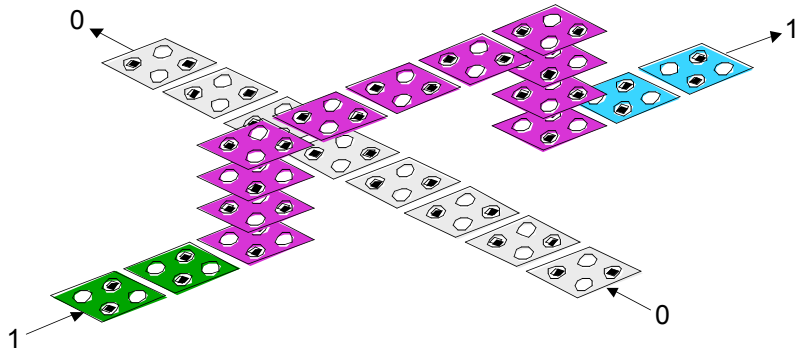
$$a \cdot b = M(a,b,0)$$

$$a + b = M(a,b,1)$$

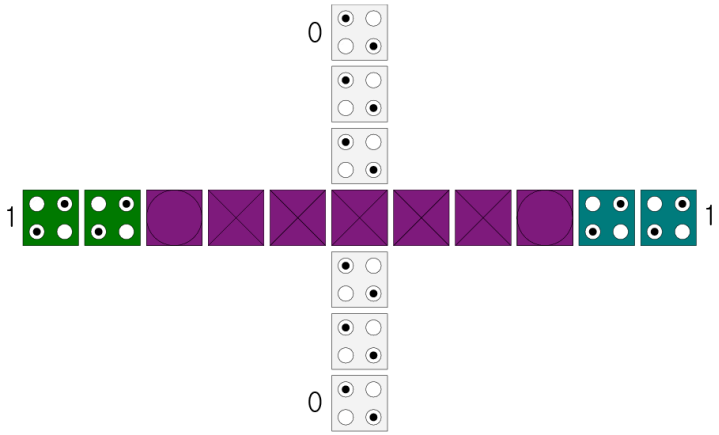
Multi-Layer Wire Crossovers

- Use Several Layers for Crossovers
  - 3D Structure
- Pros and Cons
  - \+ Area Efficient Design
  - – Manufacturability Issues

Structure



Layout



QCA Circuit Design Rules

- Cell Size
  - Set at 20nm
    - Width and Height: 18nm
    - Quantum-dot Diameter: 5nm
    - Cell Center-to-Center Spacing: 20nm
- Size Limit on Cells Per Clock Zone
  - Limit: 15 Cells
    - Proper Propagation Delay and Reliable Signal Transmission
    - Freedom for Routing and a Reasonable Clock Zone Size
- Minimum Separation of Two Different Wires
  - The Width of Two Cells
- Clock Increment Rule
  - Increment the Clock Zone at the Clock Arrangement Positions

Serial Parallel Multiplier Designs in QCA

- Multiplier Design Issues
  - A Parallel Multiplier is a Very Complex Circuit
  - Complex Circuits Often Incur Significant Delay
- Simple Structure is Desirable
  - Serial-Parallel Multiplier Design Selected
  - Filter Design Methodology is Used

Algorithmic Design

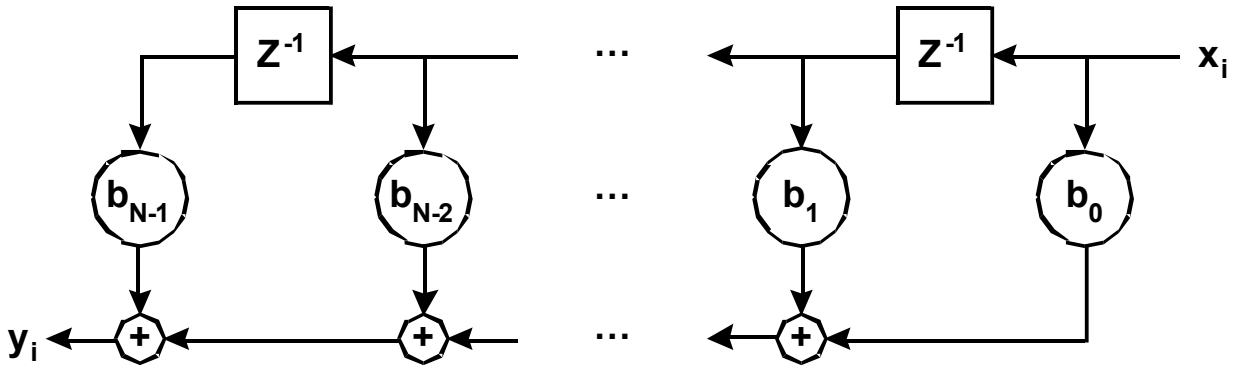
- FIR Filter Design Example
  - Delay Operator: Z^{-1}

$$Z^{-1}x_i = x_{i-1}, \quad Z^{-n} = Z^{-1}Z^{-n+1}$$

  - Filter Equation

$$y_i = b_0 x_i + b_1 x_{i-1} + b_2 x_{i-2} + \cdots + b_{N-2} x_{i-N+2} + b_{N-1} x_{i-N+1}$$

$$= \sum_{k=0}^{N-1} b_k x_{i-k} = \sum_{k=0}^{N-1} b_k Z^{-k} x_i = \left(\sum_{k=0}^{N-1} b_k Z^{-k} \right) x_i$$



Pipelined FIR Filter Network

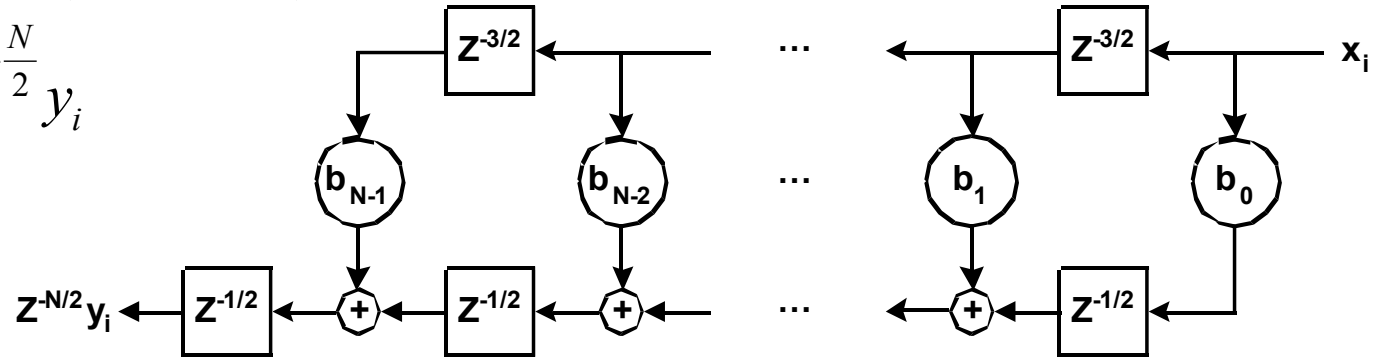
- Pipelined FIR Filter Output (Right-to-Left Structure)

$$= Z^{-\frac{1}{2}}\left(b_{N-1}Z^{-\frac{3}{2}(N-1)} + Z^{-\frac{1}{2}}\left(b_{N-2}Z^{-\frac{3}{2}(N-2)} + \cdots + Z^{-\frac{1}{2}}\left(b_0 Z^0\right)\right)\right) x_i$$

$$= Z^{-\frac{N}{2}} b_{N-1}Z^{-(N-1)}x_i + Z^{-\frac{N}{2}} b_{N-2}Z^{-(N-2)}x_i + \cdots + Z^{-\frac{N}{2}} b_0 x_i$$

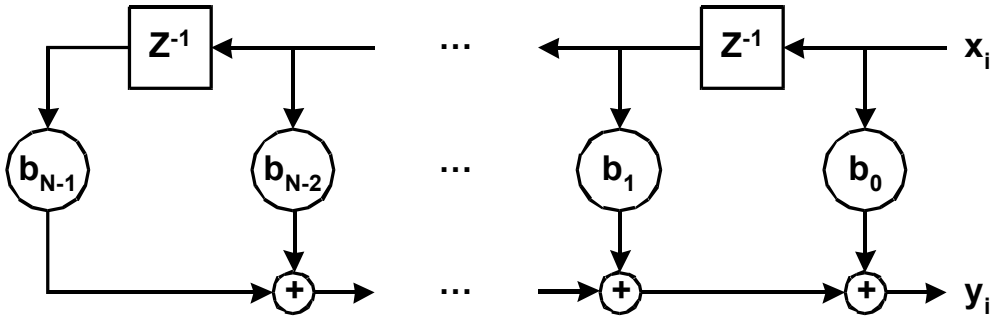
$$= Z^{-\frac{N}{2}}\left(\sum_{k=0}^{N-1} b_k Z^{-k}\right) x_i$$

$$= Z^{-\frac{N}{2}} y_i$$

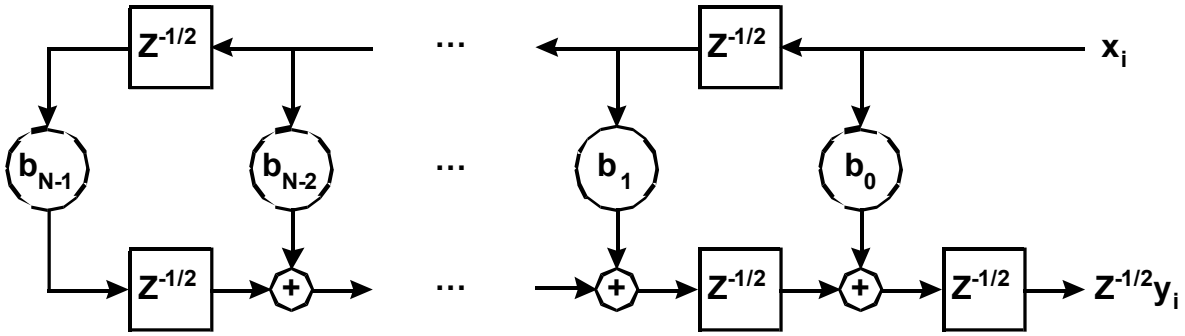


Redirected FIR Filter Network

- General Structure (Right-to-Right Structure)



- Pipelined Structure



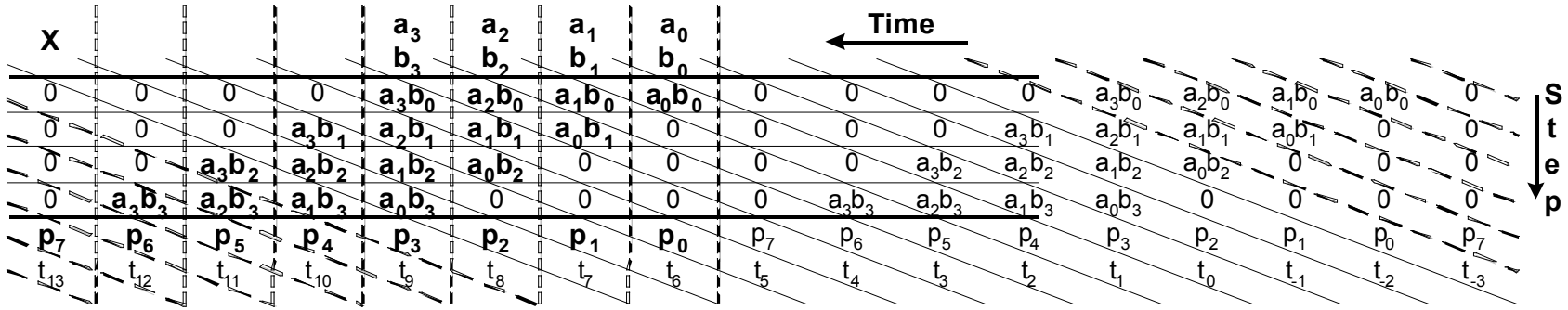
$$Z^{-\frac{1}{2}} y_i = Z^{-\frac{1}{2}} \left(\sum_{k=0}^{N-1} b_k Z^{-k} \right) x_i$$

$$= Z^{-\frac{1}{2}} \left(\sum_{k=0}^{N-1} b_k Z^{-\frac{k}{2}} Z^{-\frac{k}{2}} \right) x_i$$

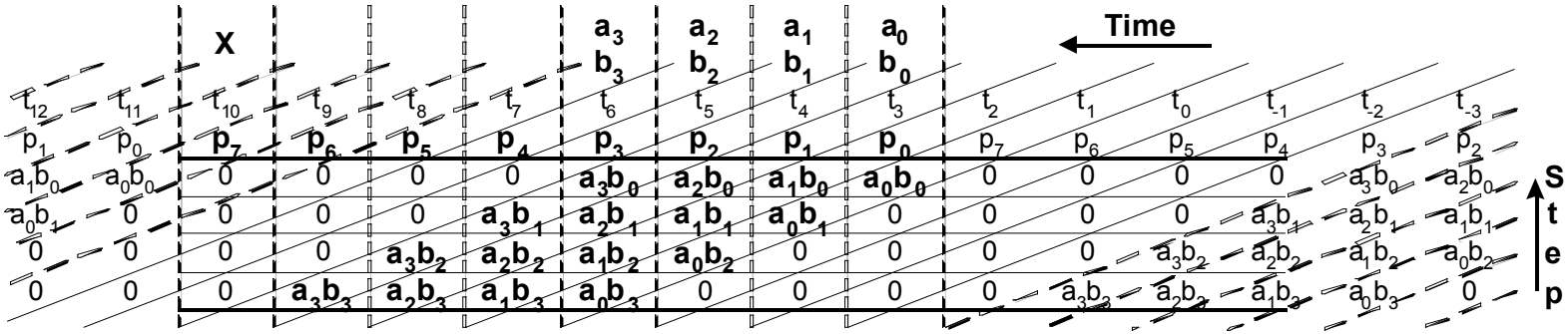
$$= Z^{-\frac{1}{2}} \left(\sum_{k=0}^{N-1} Z^{-\frac{k}{2}} b_k Z^{-\frac{k}{2}} \right) x_i$$

Multiplication Signal Flows

- Unsigned Number Multiplication
  - Bit Product Matrix and Signal Flow of Right-to-Left Structure

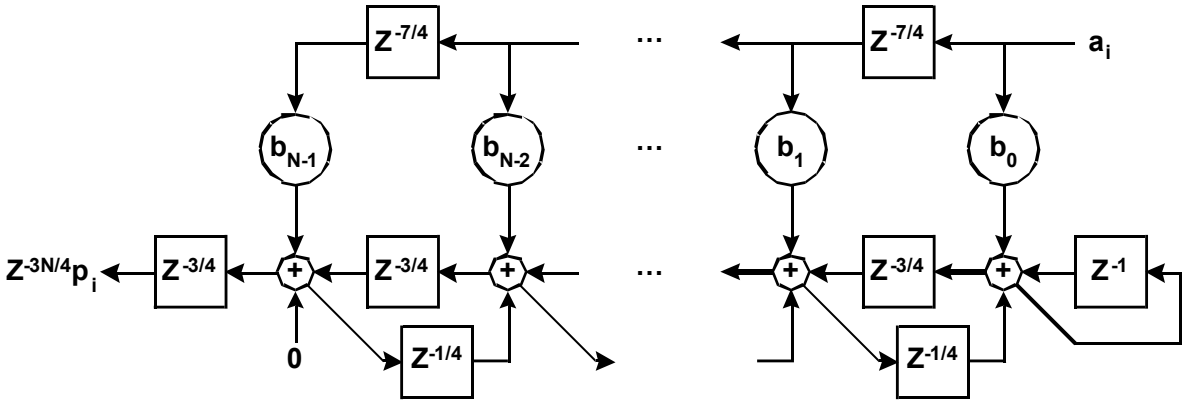


  - Bit Product Matrix and Signal Flow of Right-to-Right Structure

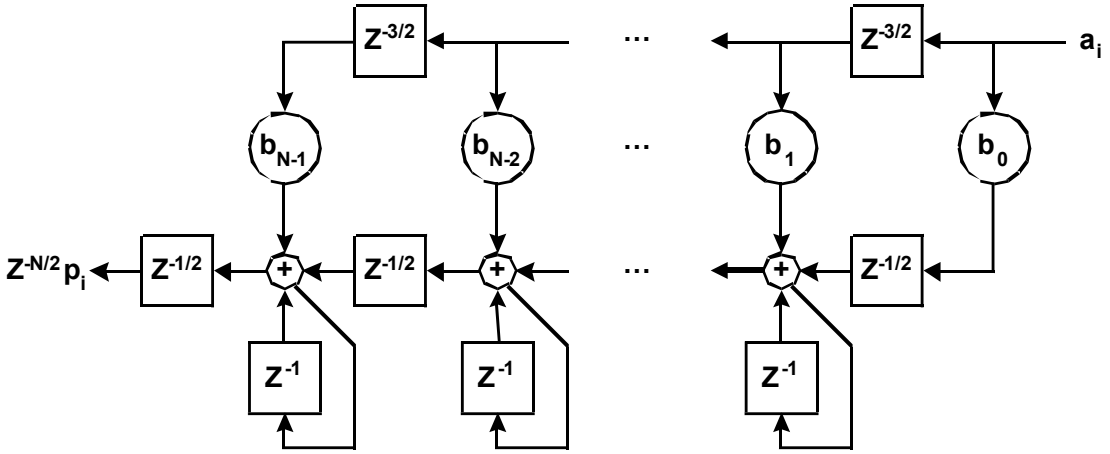


Network Diagrams-I

- Right-to-Left Carry Shift Multiplication (CSM)

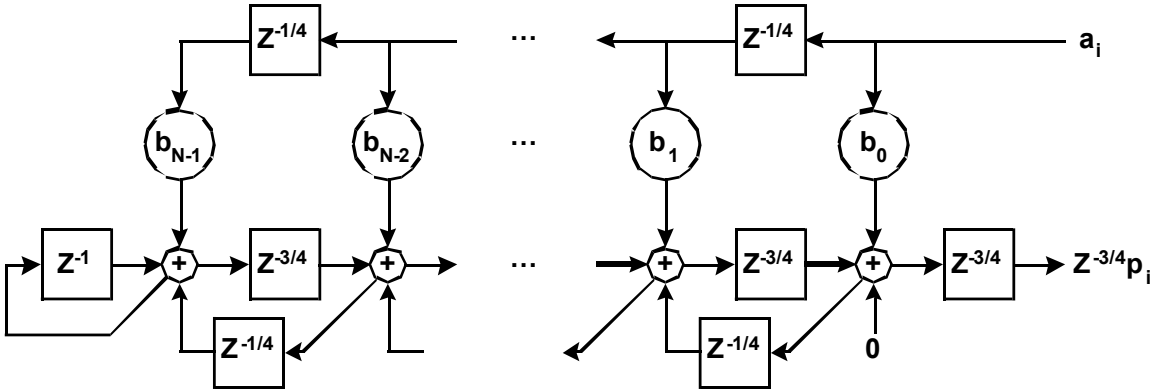


- Right-to-Left Carry Delay Multiplication (CDM)

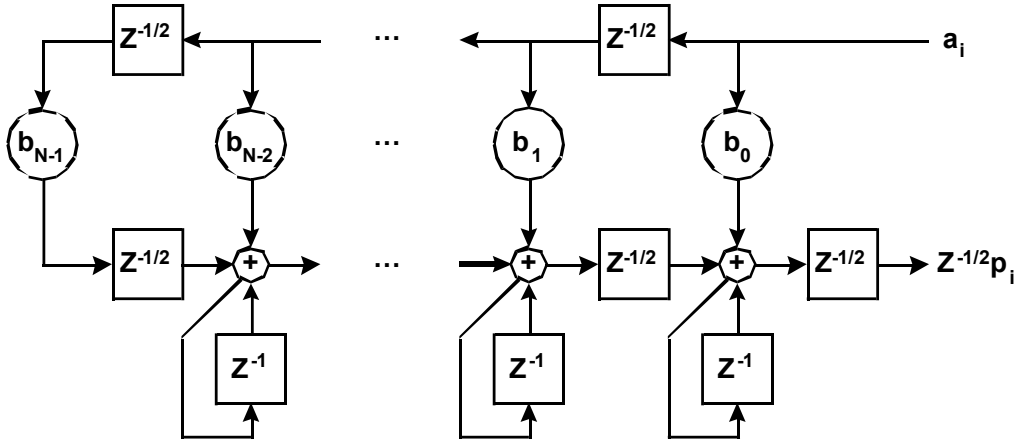


Network Diagrams-II

- Right-to-Right Carry Shift Multiplication (CSM)

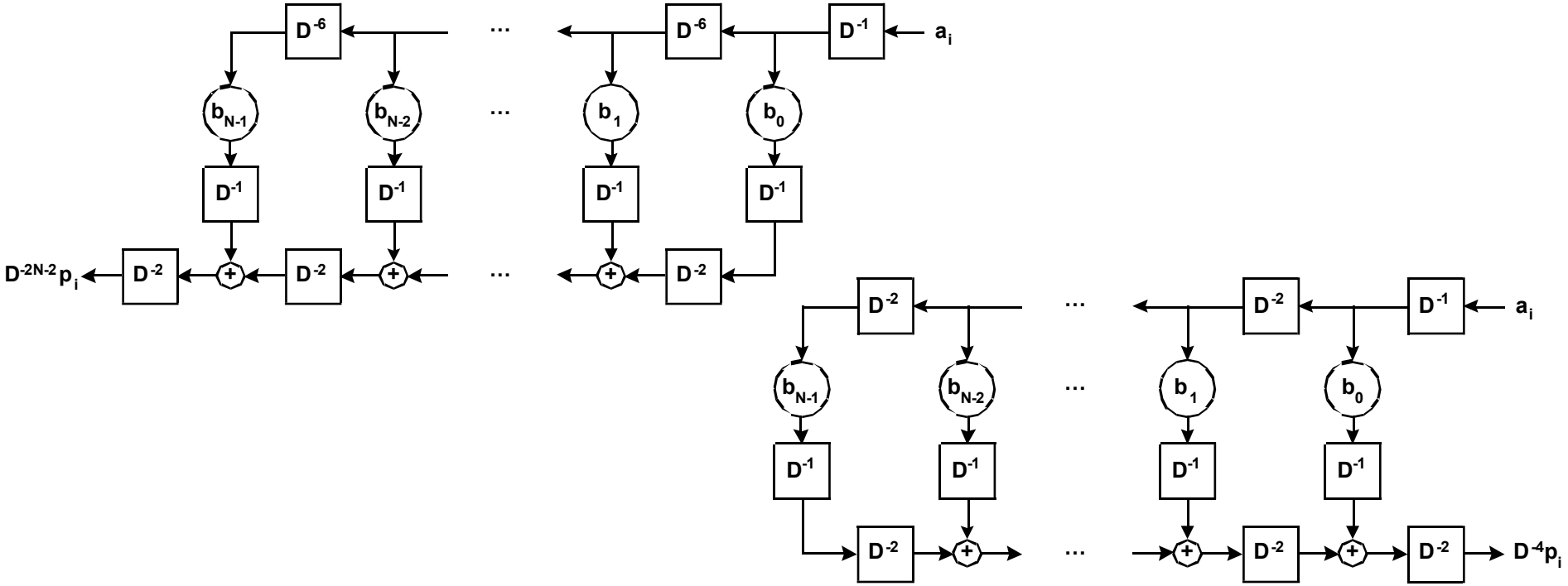


- Right-to-Right Carry Delay Multiplication (CDM)



QCA Multiplication Diagrams

- Multiplication Networks for QCA
  - One Clock Zone Delay: D^{-1} ($D^{-4}=Z^{-1}$)
- Filter Network Transformation Using D Operators



Right-to-Left Networks

- Equations

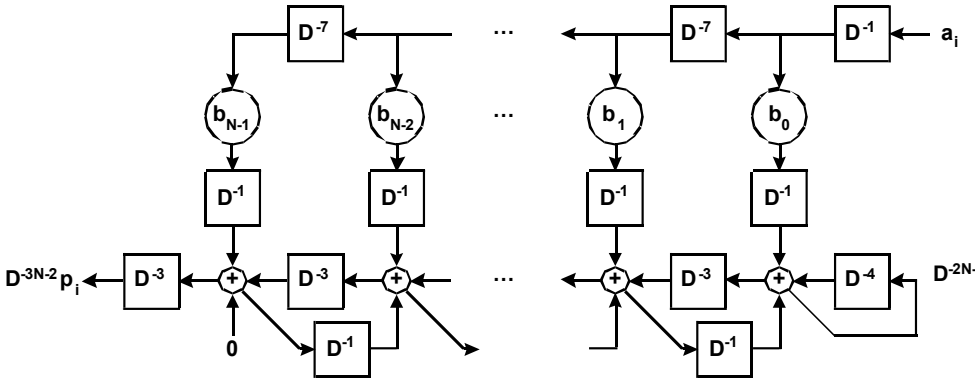
$$(s_{ij}, c_{ij}) = \text{Addition}\left(b_j D^{-7j-2} a_i, D^{-3} s_{i(j-1)}, D^{-1} c_{i(j+1)}\right)$$

$$= \text{Addition}\left(b_j a_{i-7j-2}, s_{(i-3)(j-1)}, c_{(i-1)(j+1)}\right)$$

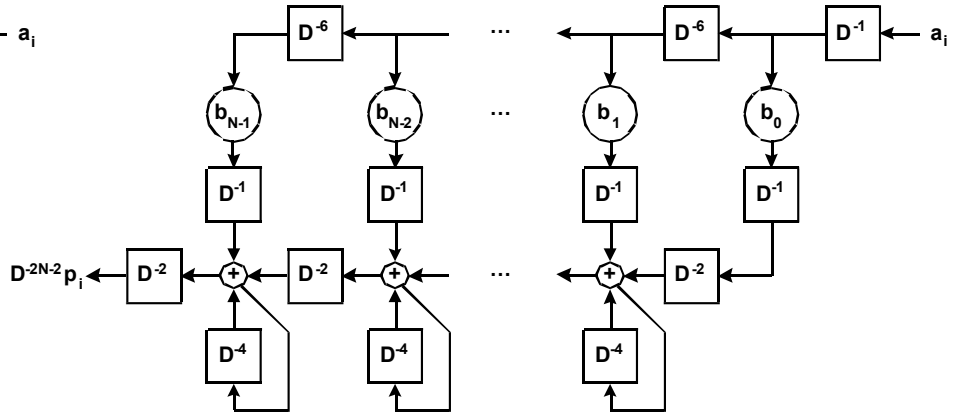
$$(s_{ij}, c_{ij}) = \text{Addition}\left(b_j D^{-6j-2} a_i, D^{-2} s_{i(j-1)}, D^{-4} c_{ij}\right)$$

$$= \text{Addition}\left(b_j a_{i-6j-2}, s_{(i-2)(j-1)}, c_{(i-4)j}\right)$$

CSM Network



CDM Network



Right-to-Right Networks

- Equations

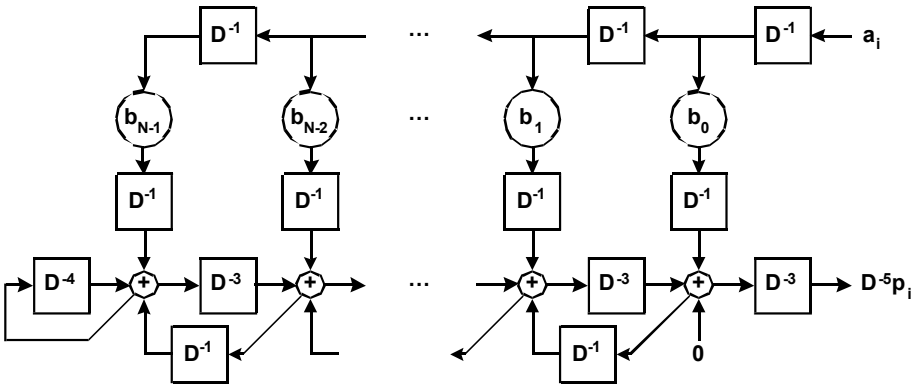
$$(s_{ij}, c_{ij}) = \text{Addition}\left(b_j D^{-j-2} a_i,\ D^{-3} s_{i(j+1)},\ D^{-1} c_{i(j-1)}\right)$$

$$= \text{Addition}\left(b_j a_{i-j-2},\ s_{(i-3)(j+1)},\ c_{(i-1)(j-1)}\right)$$

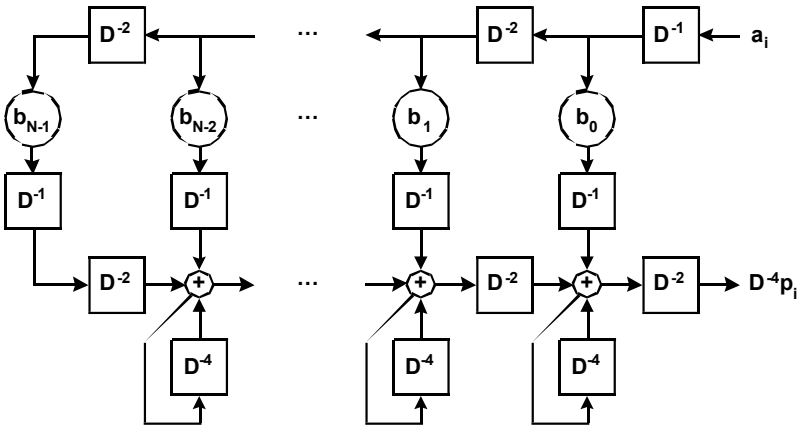
$$(s_{ij}, c_{ij}) = \text{Addition}\left(b_j D^{-2j-2} a_i,\ D^{-2} s_{i(j+1)},\ D^{-4} c_{ij}\right)$$

$$= \text{Addition}\left(b_j a_{i-2j-2},\ s_{(i-2)(j+1)},\ c_{(i-4)j}\right)$$

CSM Network

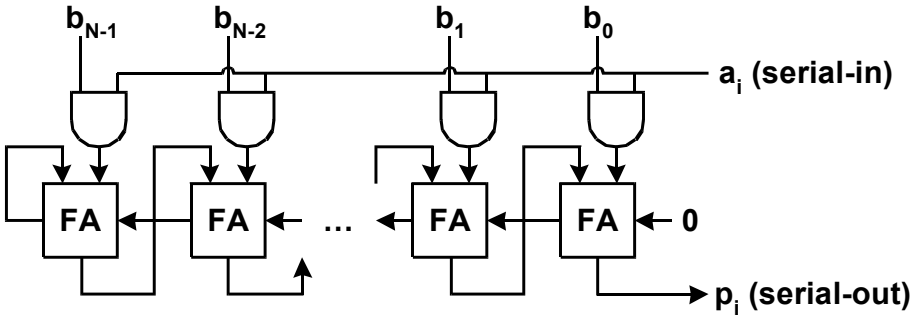


CDM Network

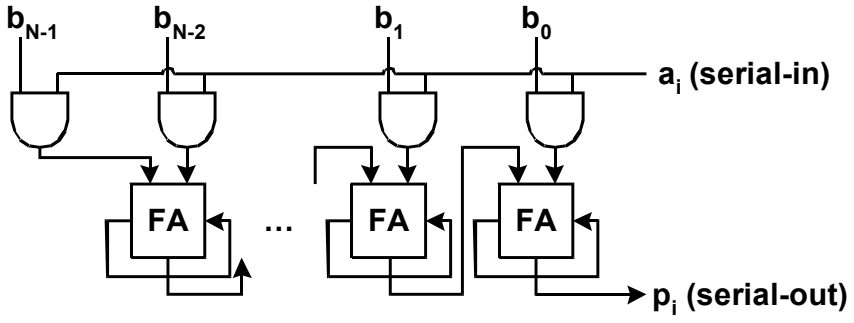


Multiplier Block Diagrams

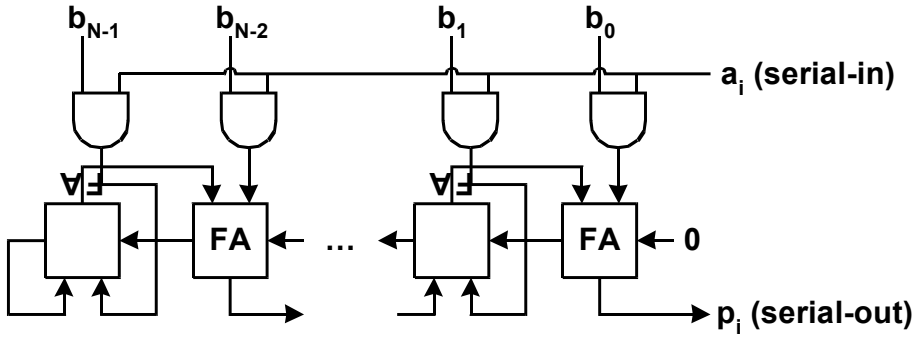
- Nominal Design
  - Right-to-Right CSM

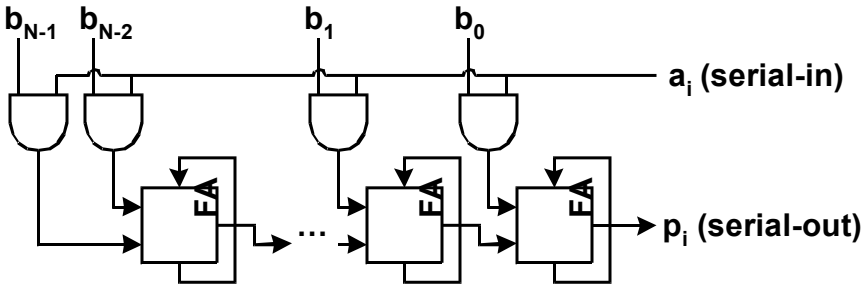


  - Right-to-Right CDM

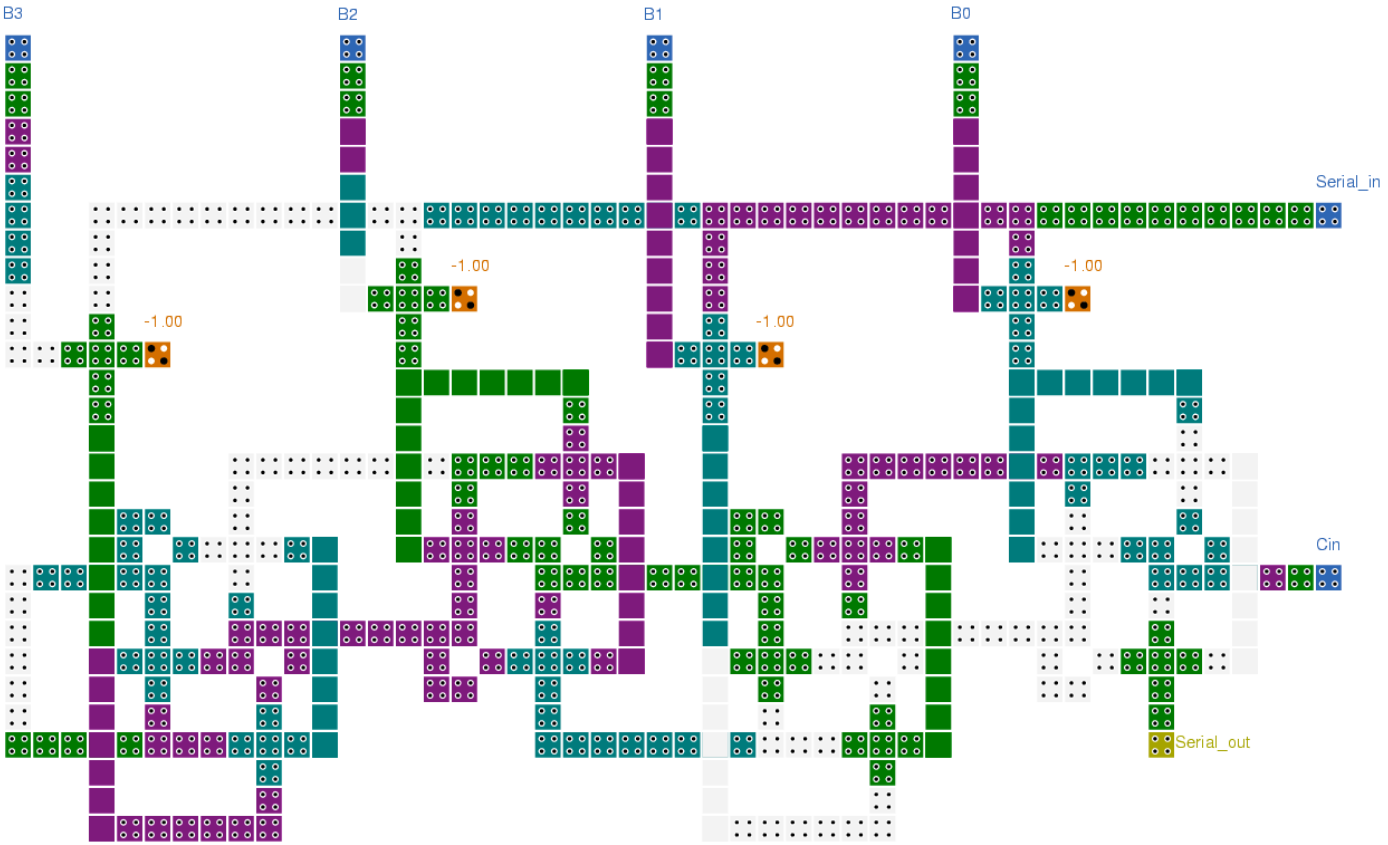


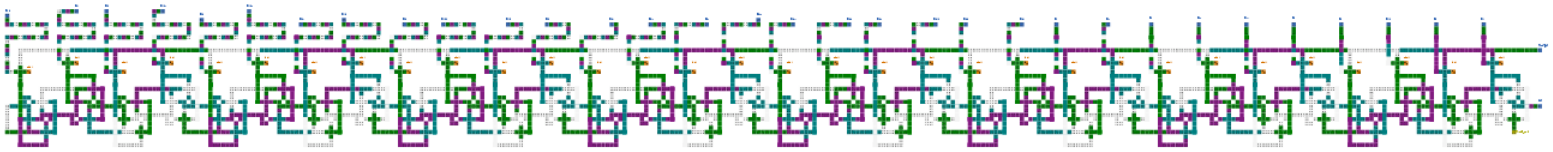
Modified Design



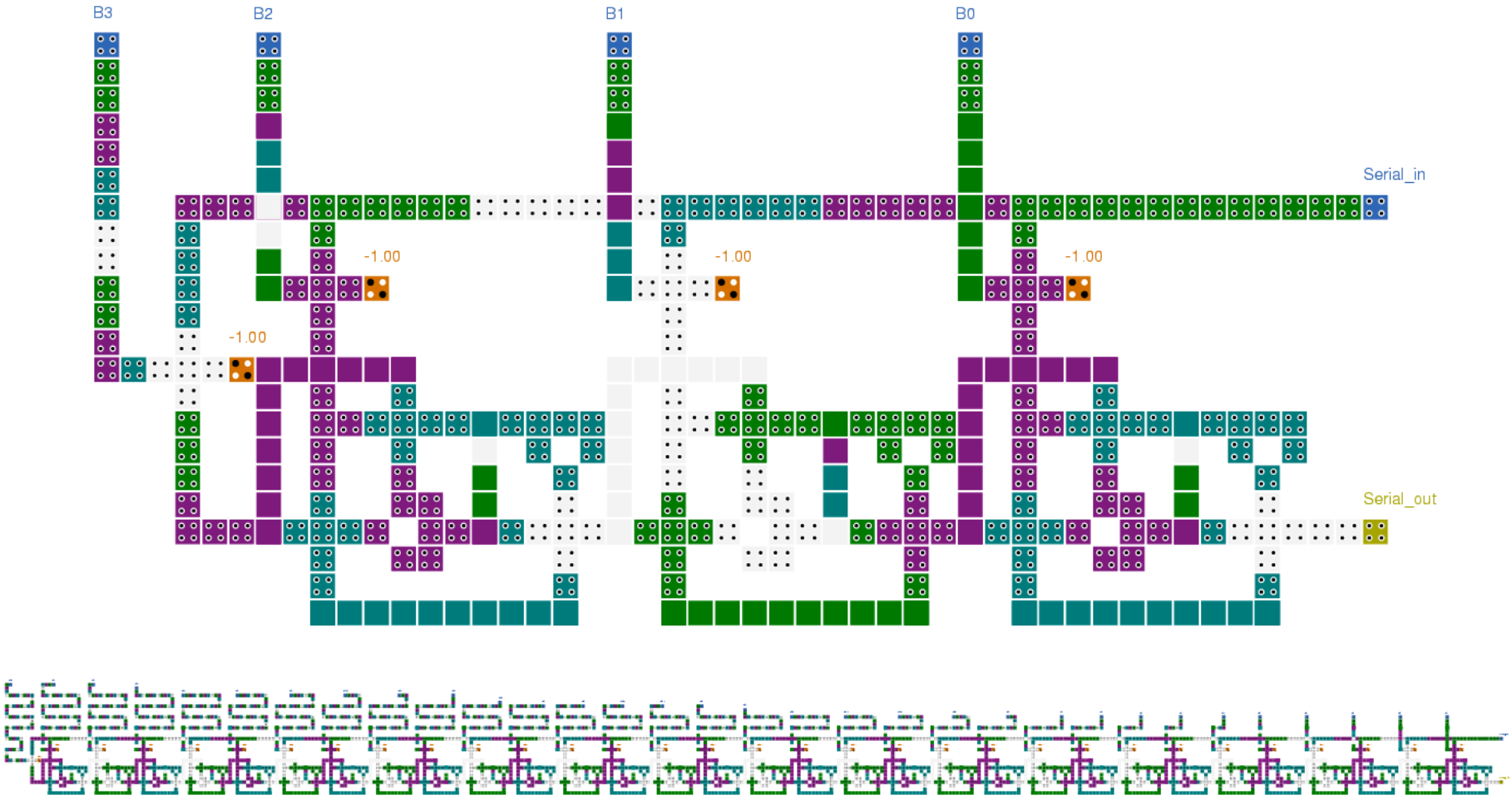


4-bit and 32-bit CSM Layouts



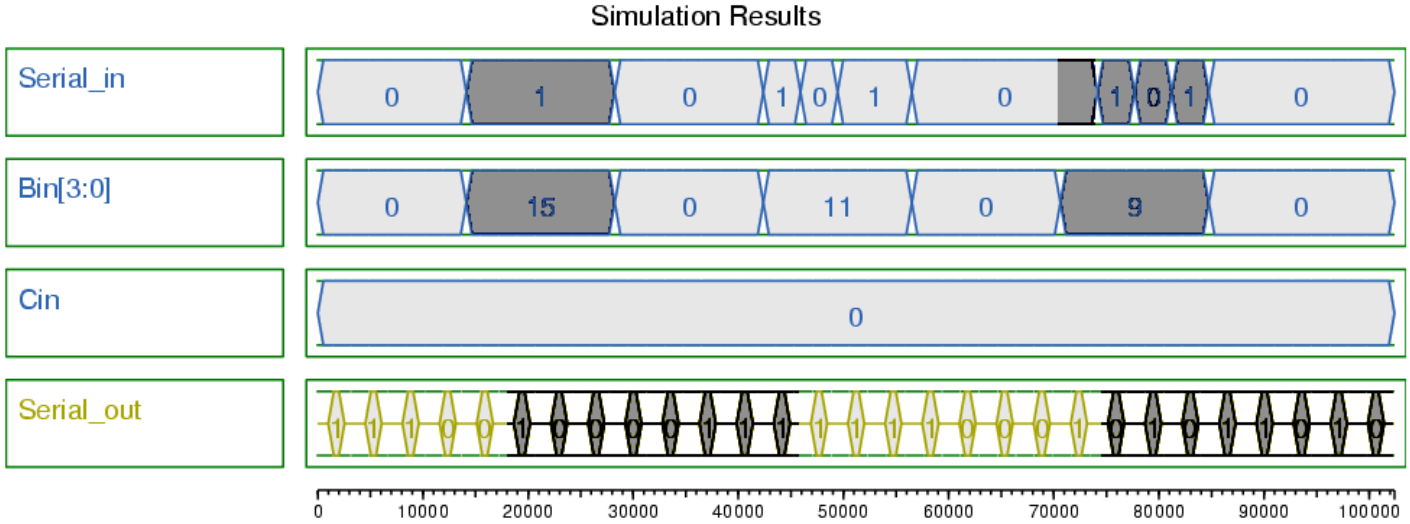


4-bit and 32-bit CDM Layouts

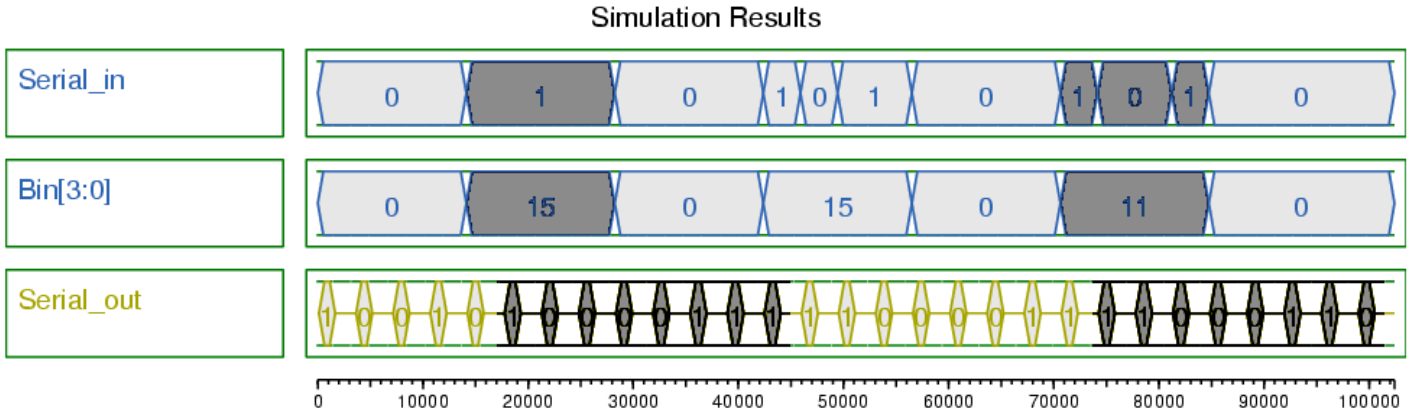


4-bit CSM and CDM Simulation Results

- CSM Results



- CDM Results



Carry Shift Multipliers

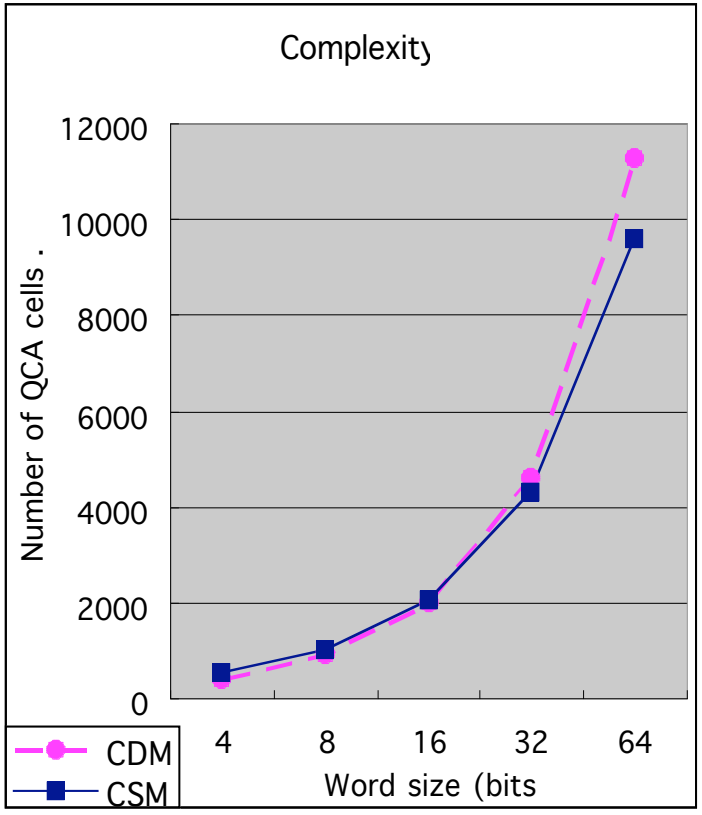
Size	Complexity	Area	Latency
CSM-4	507 cells	1.04 μm x 0.61 μm	1.25 clocks
CSM-8	1,011 cells	1.93 μm x 0.61 μm	1.25 clocks
CSM-16	2,043 cells	3.67 μm x 0.61 μm	1.25 clocks
CSM-32	4,299 cells	7.24 μm x 0.67 μm	1.25 clocks
CSM-64	9,579 cells	14.3 μm x 0.85 μm	1.25 clocks

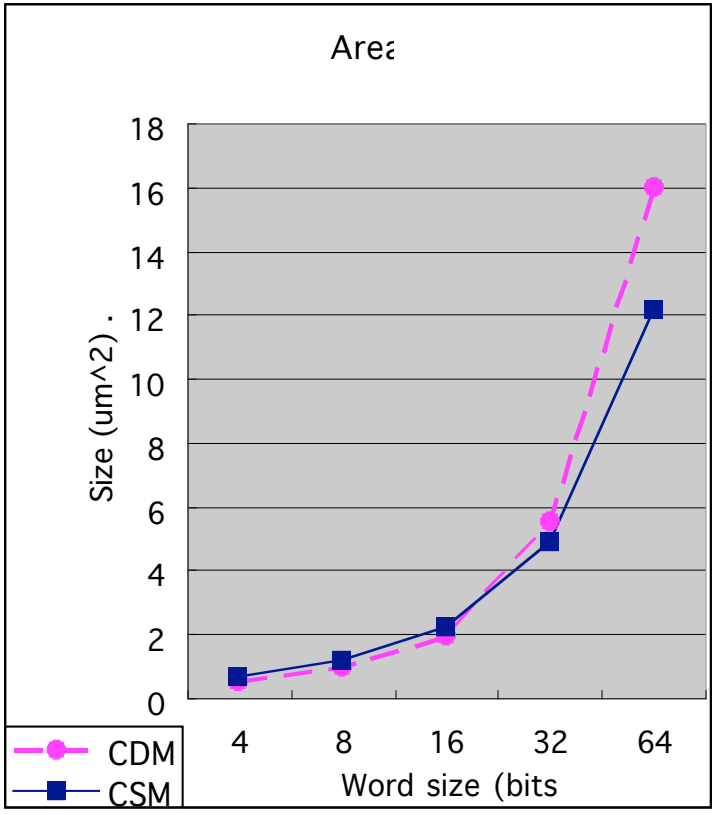
Carry Delay Multipliers

Size	Complexity	Area	Latency
CDM-4	406 cells	1.05 μm x 0.47 μm	1 clock
CDM-8	903 cells	2.12 μm x 0.47 μm	1 clock
CDM-16	1,999 cells	4.19 μm x 0.47 μm	1 clock
CDM-32	4,575 cells	8.47 μm x 0.65 μm	1 clock
CDM-64	11,264 cells	16.8 μm x 0.95 μm	1 clock

Comparison of Different Multipliers

- Multiplier Comparisons
  - Delay: CSM=1.25 clocks, CDM=1 clock





Conclusions

- Summary
  - Serial Parallel Multiplier Architecture
    - Simple Structure Chosen for Wire Delay Minimization
    - Regular Cells for Design Reuse
    - Optimized to Minimize Latency
  - Serial Parallel Multiplication Network
    - Based on Filter Network Example
    - Derived the Equations and Network Graph
  - Designed Two Serial Parallel Multipliers
    - Carry Shift Multiplier and Carry Delay Multiplier
- Contributions
  - Extended QCA Circuit Designs to Multiplication
  - Explored Various Serial Parallel Multiplication Algorithms

QUESTIONS???