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Return of the hardware floating-point elementary functions

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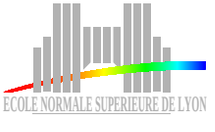
http://www.ens-lyon.fr/LIP/Arenaire/


Outline of the talk

- Context
- Double-precision exponential
- Results
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  - M. D. Ercegovac (IEEE TC, 1975)
    Radix-16 evaluation of certain elementary functions.
  - G. Paul and M. W. Wilson (ACM TOMS, 1976)
    Should the elementary functions be incorporated into computer instruction sets?
  - C. Wrathall and T. C. Chen. (ARITH 4, 1978)
    Convergence guarantee and improvements for a hardware exponential and logarithm evaluation scheme.
  - P. Farmwald (ARITH 5, 1981)
    High-bandwidth evaluation of elementary functions.
  - M. Cosnard, A. Guyot, B. Hochet, J.-M. Muller, H. Ouaouicha, P. Paul, and E. Zysmann (ARITH 8, 1987)
    The FELIN arithmetic coprocessor chip.

FPUs strike back

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  - dedicated efficient hardware operators
  - only basic operations: $+$, $-$, $\times$, $\div$ and $\sqrt{\ }$

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- only software or micro-code implementations

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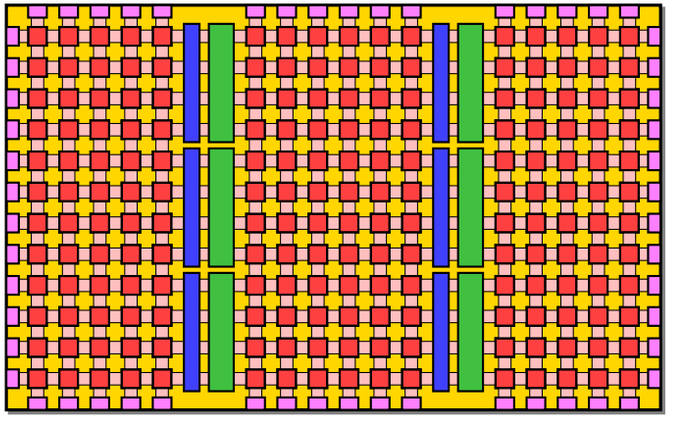
- architecture based on programmable logic cells and routing resources
  - lower performances than ASICs
  - high flexibility
  - fine-grain parallelism
  - lower cost per unit



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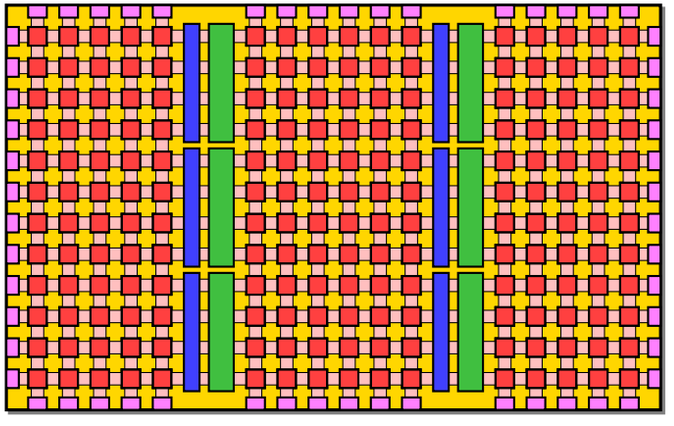

- 1 billion transistor FPGAs: huge computational capacity
- many application domains:
  - digital signal and image processing
  - cryptography
  - bioinformatics
  - scientific computing
  - ...

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- table-based method for the actual computation
  - exponential growth of the area
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- need for another algorithm, suited to higher precisions
- iterative method
  - smaller architecture
  - higher scalability
  - longer critical path

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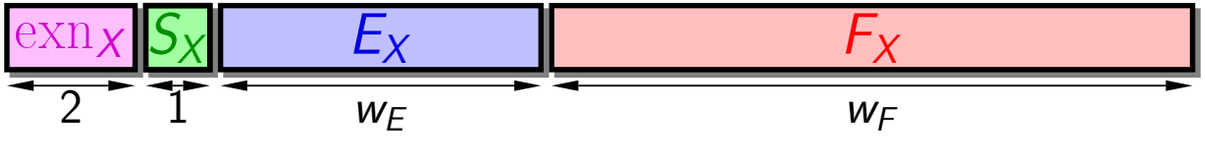
Number format

- 2 parameters: w_E (range) and w_F (precision)
- inspired from the IEEE-754 standard:

$$X = (-1)^{S_X} \cdot 1.F_X \cdot 2^{E_X - E_0}$$

Number format



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- 2 extra bits for exceptional cases: zero, infinity or *Not-a-Number* (NaN)

Evaluation method

- range reduction:

$$X = k \cdot \log 2 + Y \qquad \text{with } k \in \mathbb{Z} \text{ and } 0 \leq Y < 1$$

- we obtain:

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- fixed-point e^Y?
  generalization of an idea by Wong and Goto (IEEE TC 1994)
  - successive range reductions of the fixed-point argument Y
  - once the argument sufficiently reduced, direct evaluation of the exponential
  - reconstructions using rectangular multipliers
  - computes $e^Y - 1$

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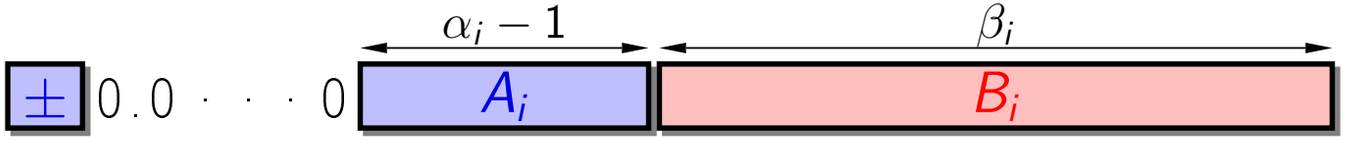

- splitting Y_i as $A_i + B_i$, we address two look-up tables with A_i:
  - $e^{A_i} - 1$, rounded to its α_i most significant bits, noted $\widetilde{e^{A_i}} - 1$
  - $L_i = \log\left(\widetilde{e^{A_i}}\right)$, rounded to its $\alpha_i + \beta_i$ most significant bits

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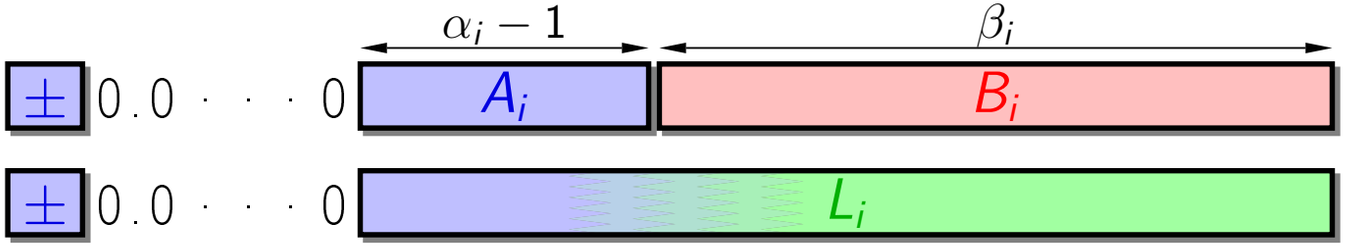

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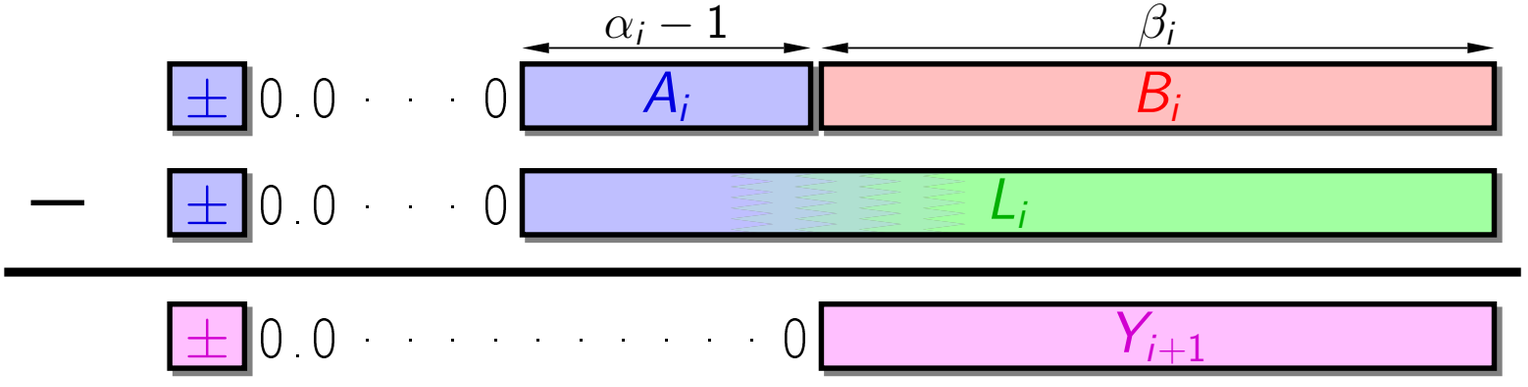

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- by construction, $L_i \approx Y_i$
- we then define Y_{i+1} as $Y_i - L_i$:
  - the $\alpha_i - 1$ most significant bits of Y_i are cancelled
  - Y_{i+1} is a $1 + \beta_i$-bit number

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- the reduction process is iterated until the step k such that

$$Y_k < 2^{-\lceil w_F/2 \rceil}$$

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- we can then approximate the exponential as

$$e^{Y_k} - 1 \approx Y_k$$

Iterative method: reconstructions

- at each step i, we have:
  - $\widetilde{e^{A_i}} - 1$, from the corresponding range reduction step
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$$\left(\widetilde{e^{A_i}} - 1\right) \times \left(e^{Y_{i+1}} - 1\right) + \left(\widetilde{e^{A_i}} - 1\right) + \left(e^{Y_{i+1}} - 1\right)$$

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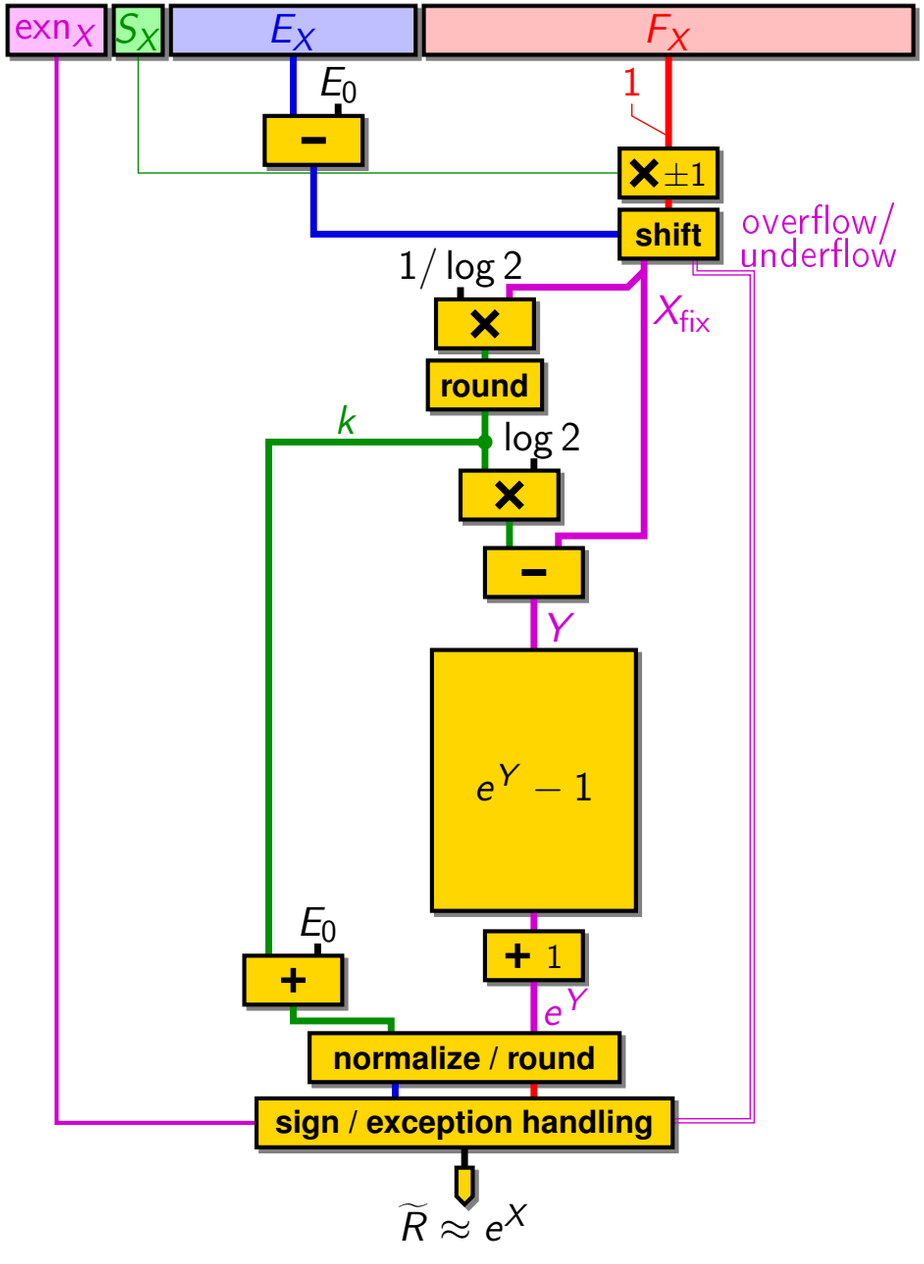
Architecture



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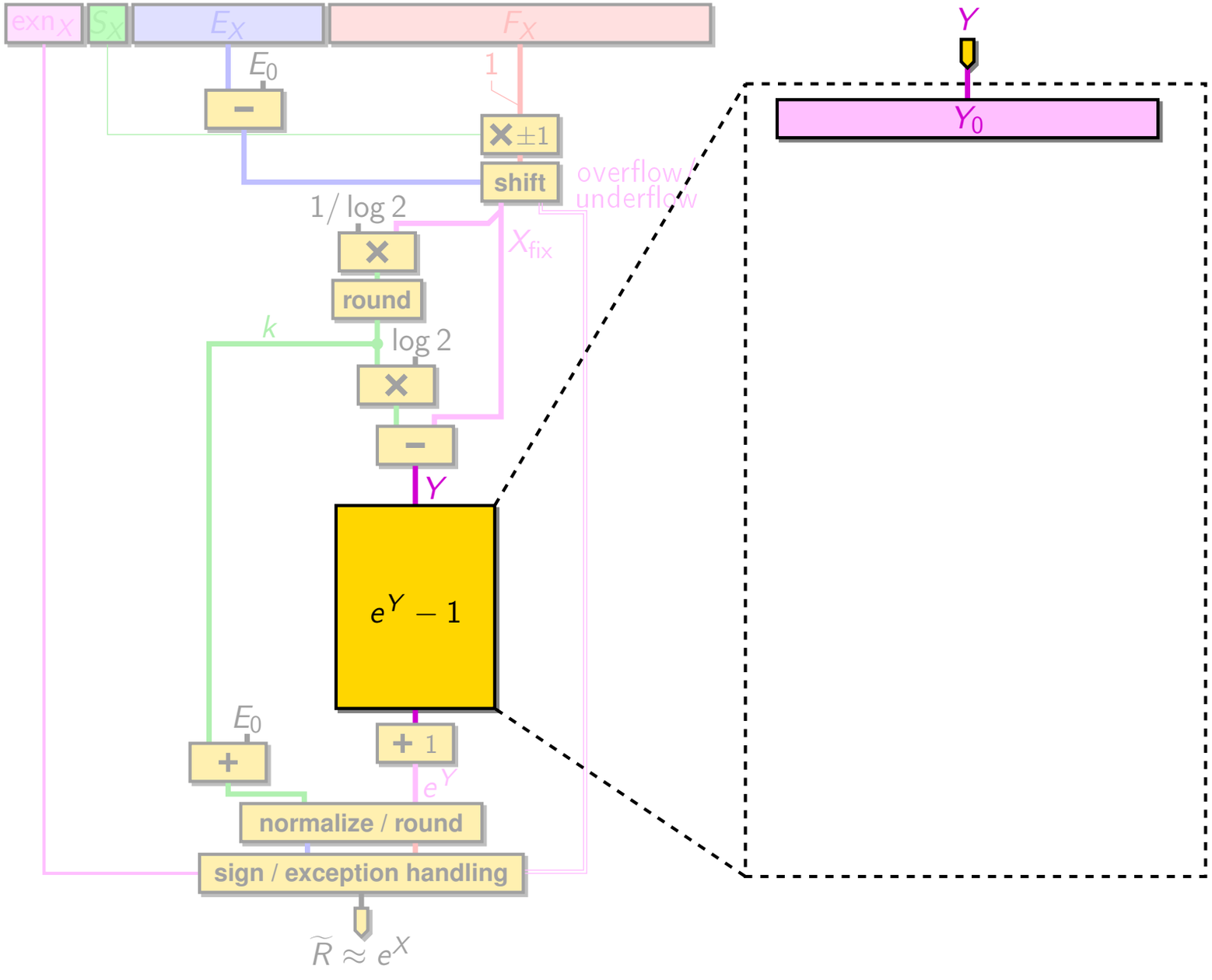

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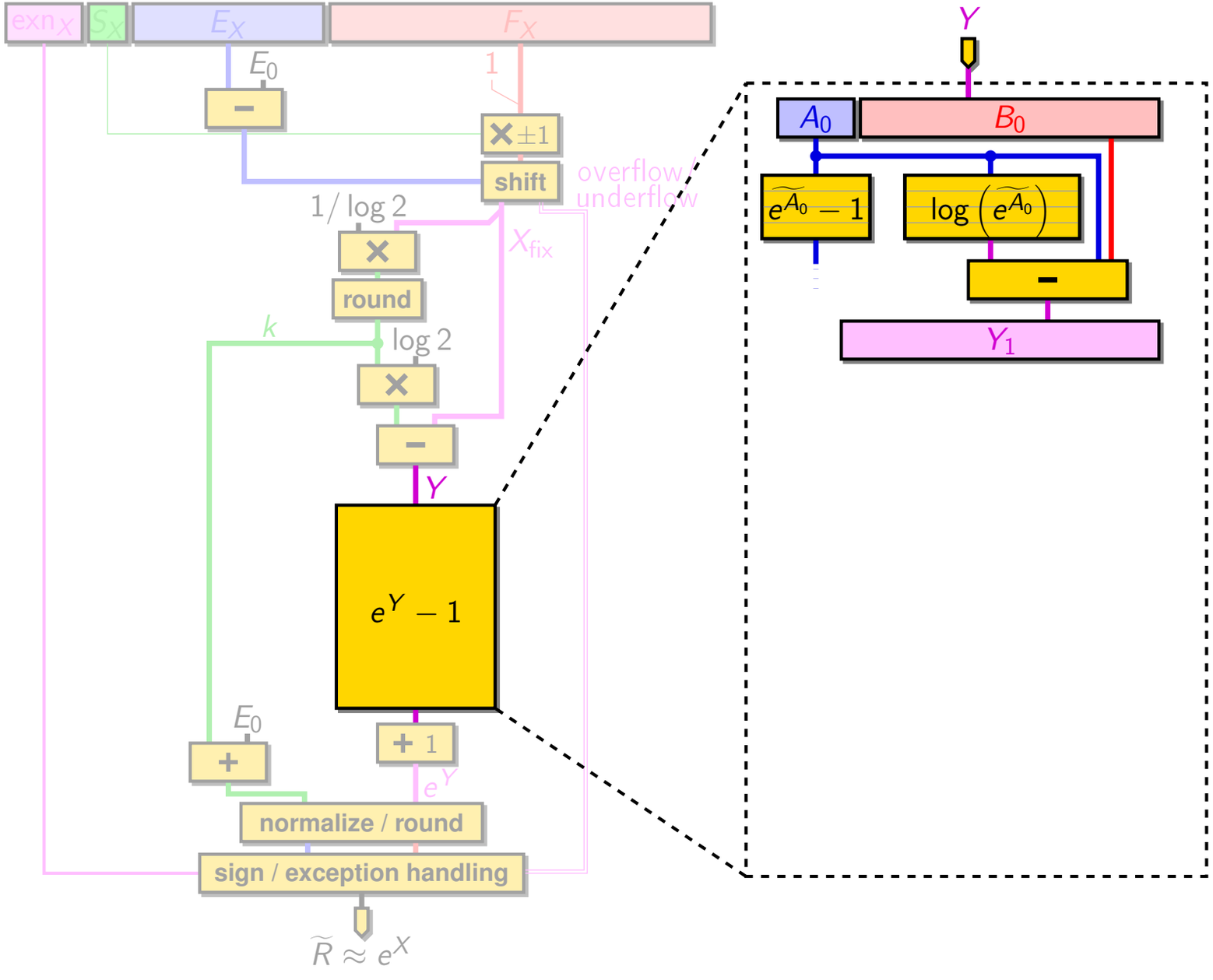

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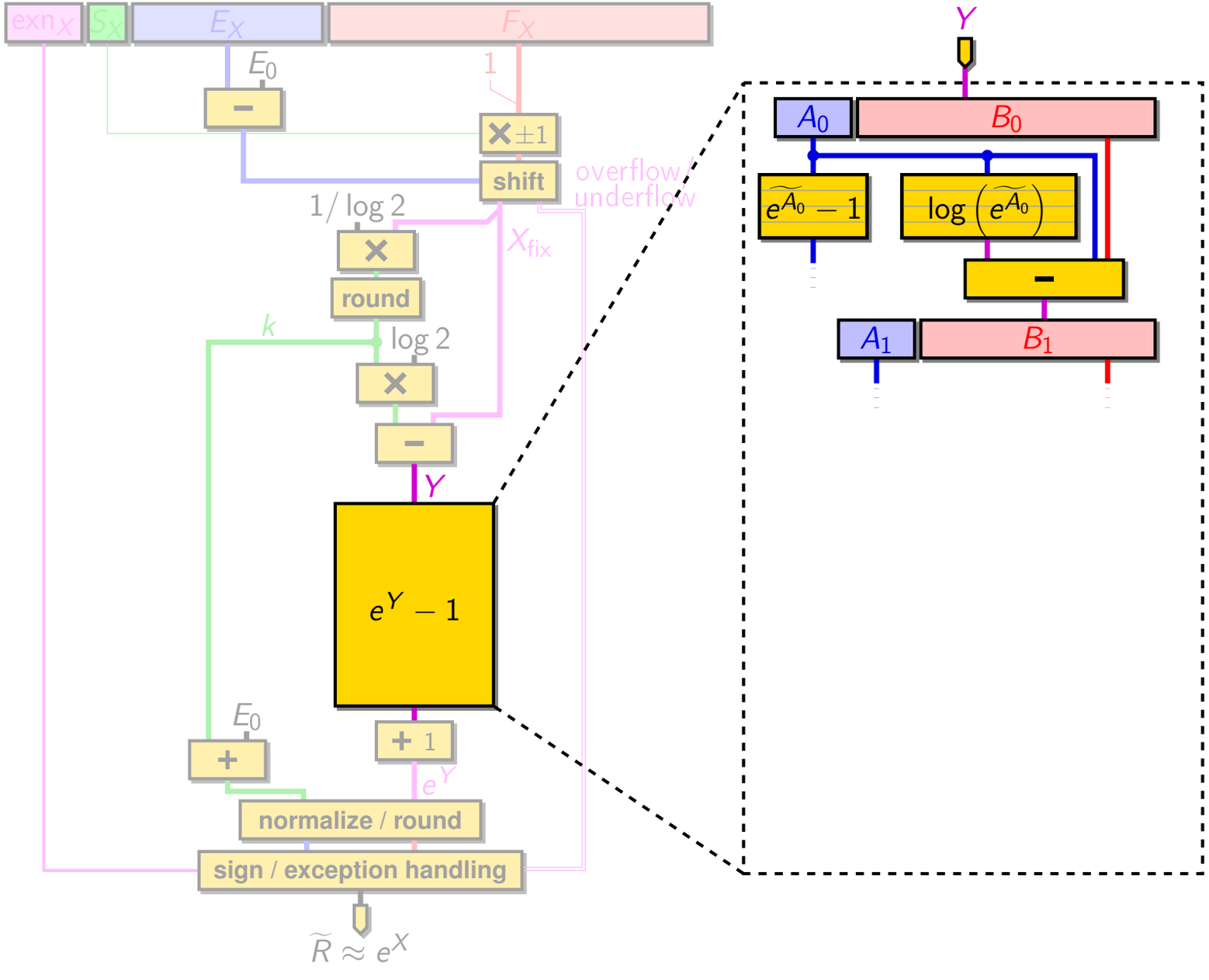

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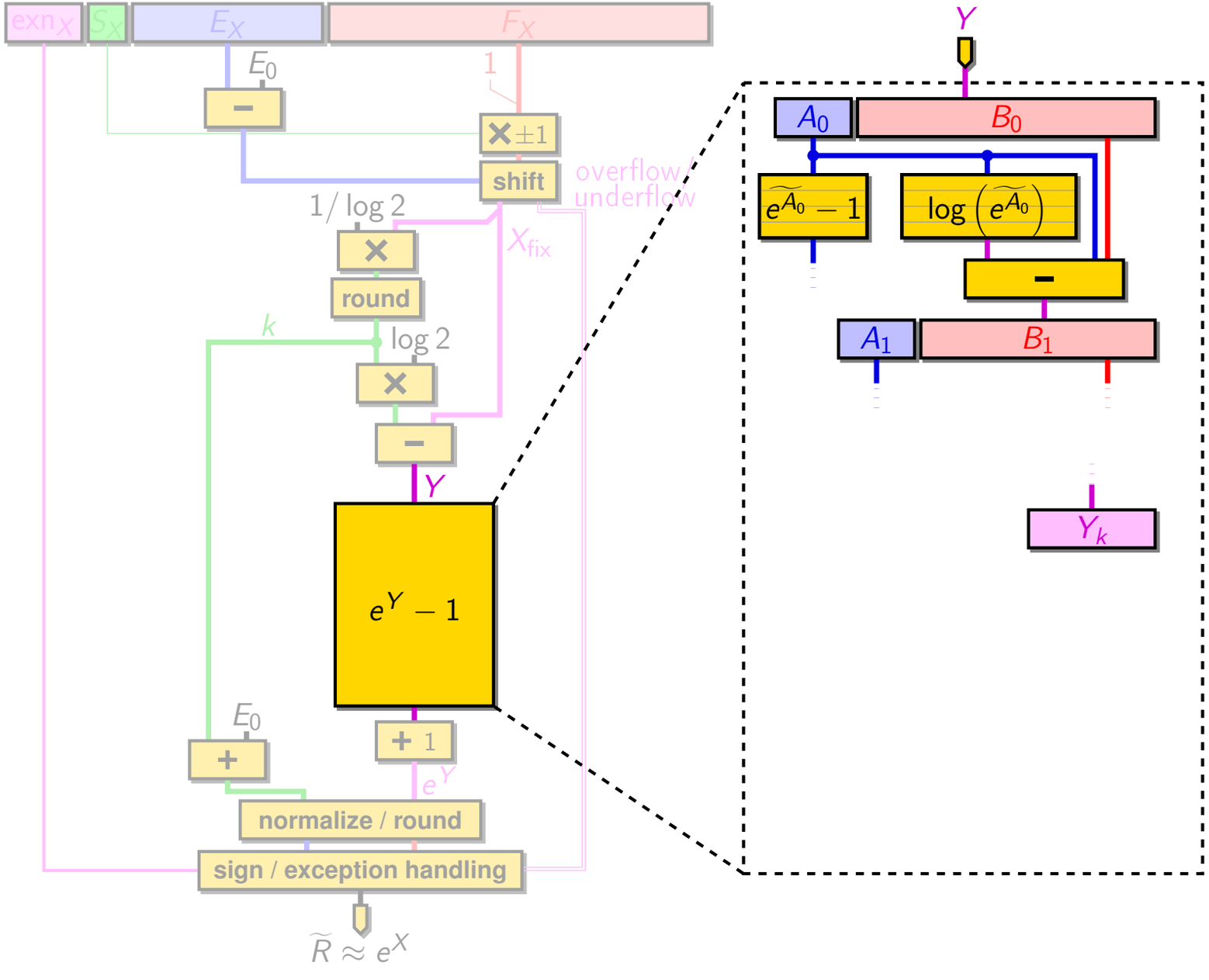

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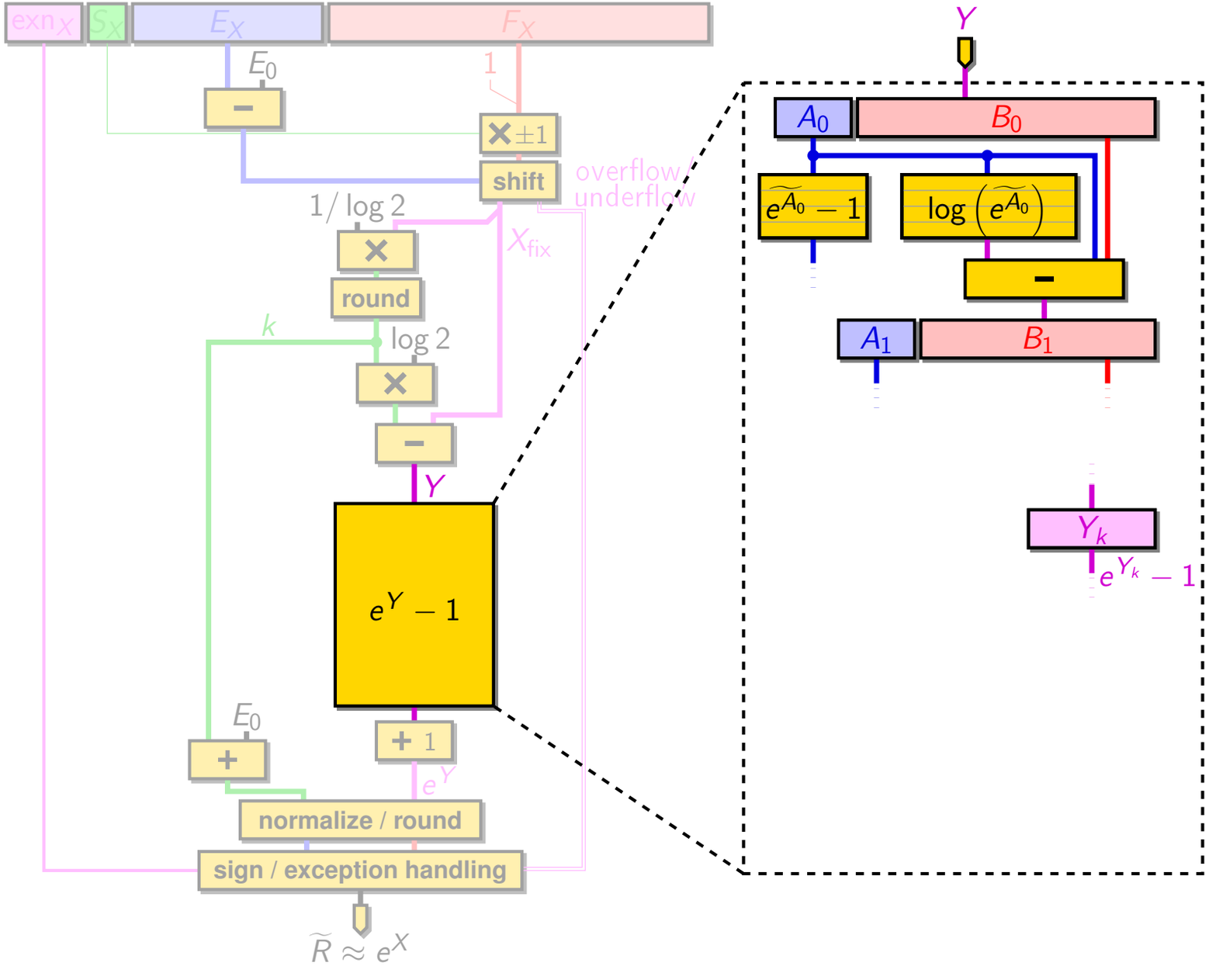

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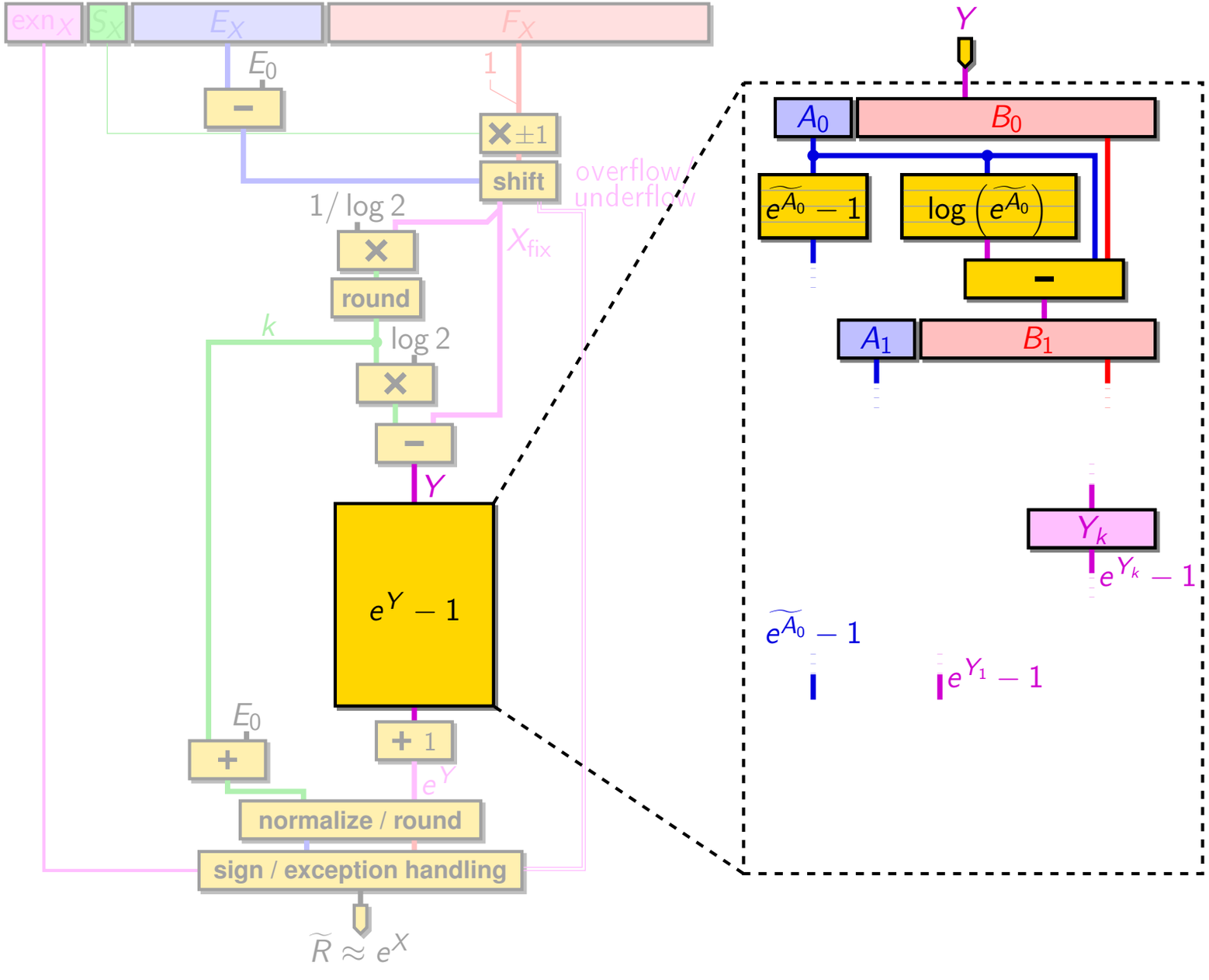

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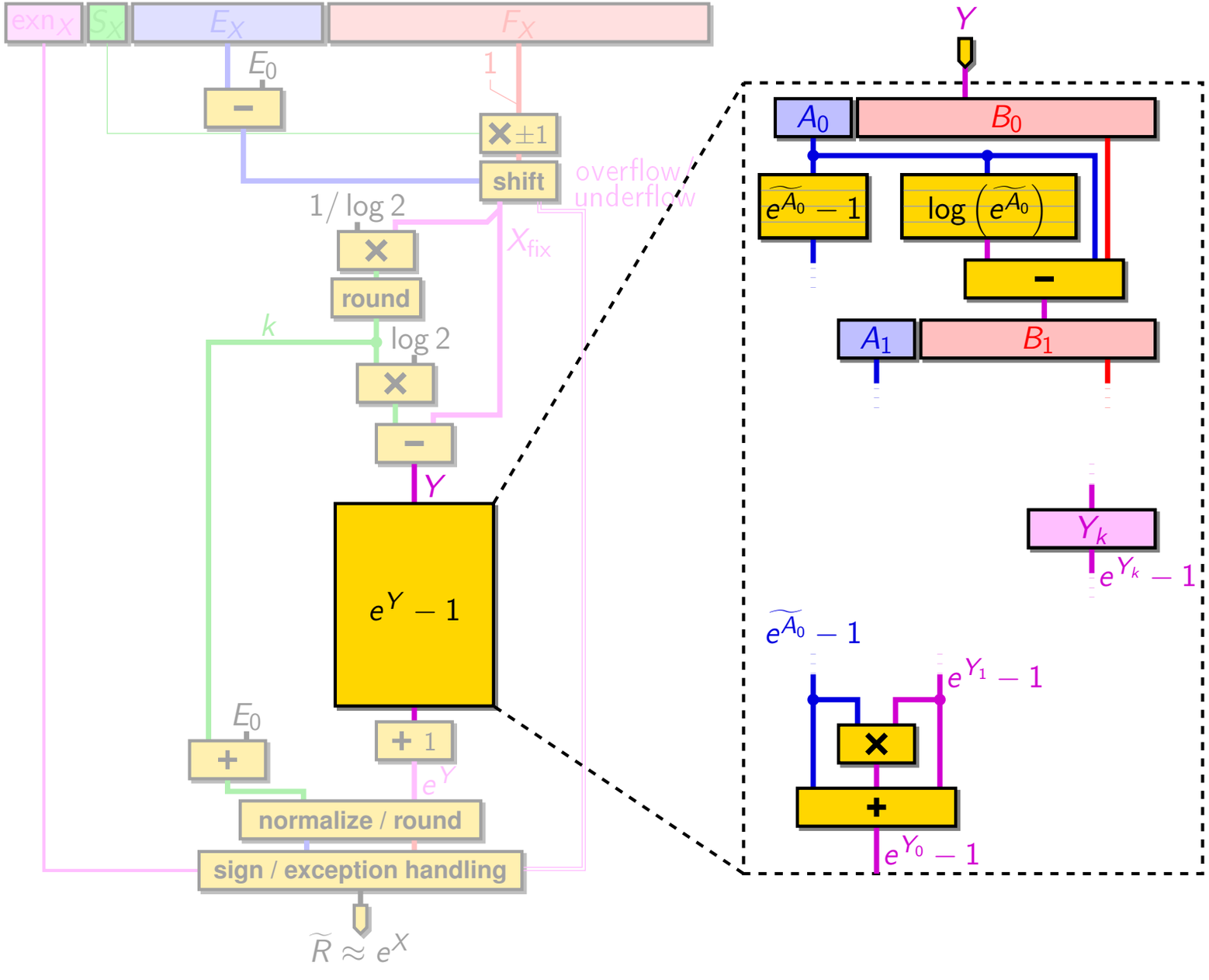

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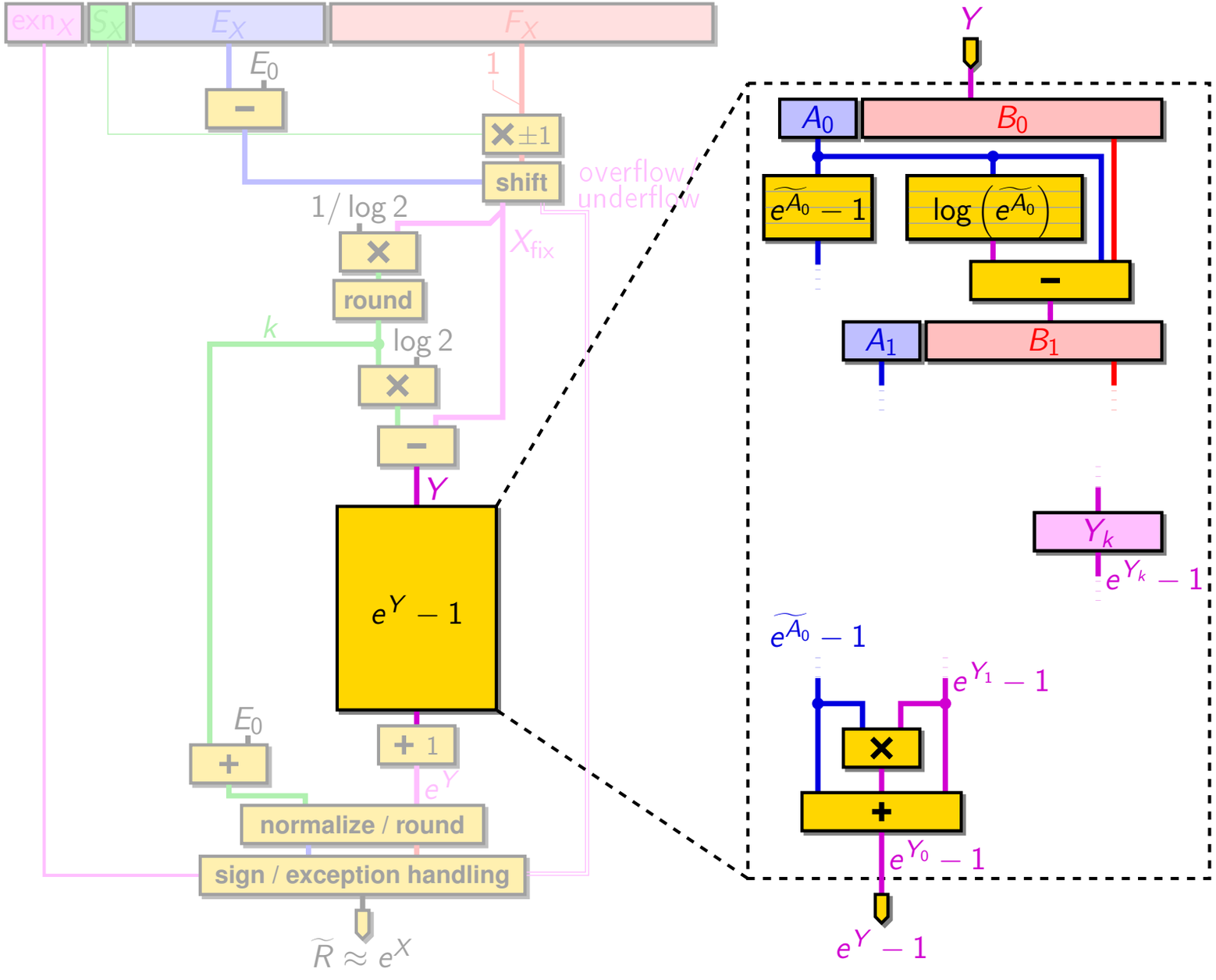

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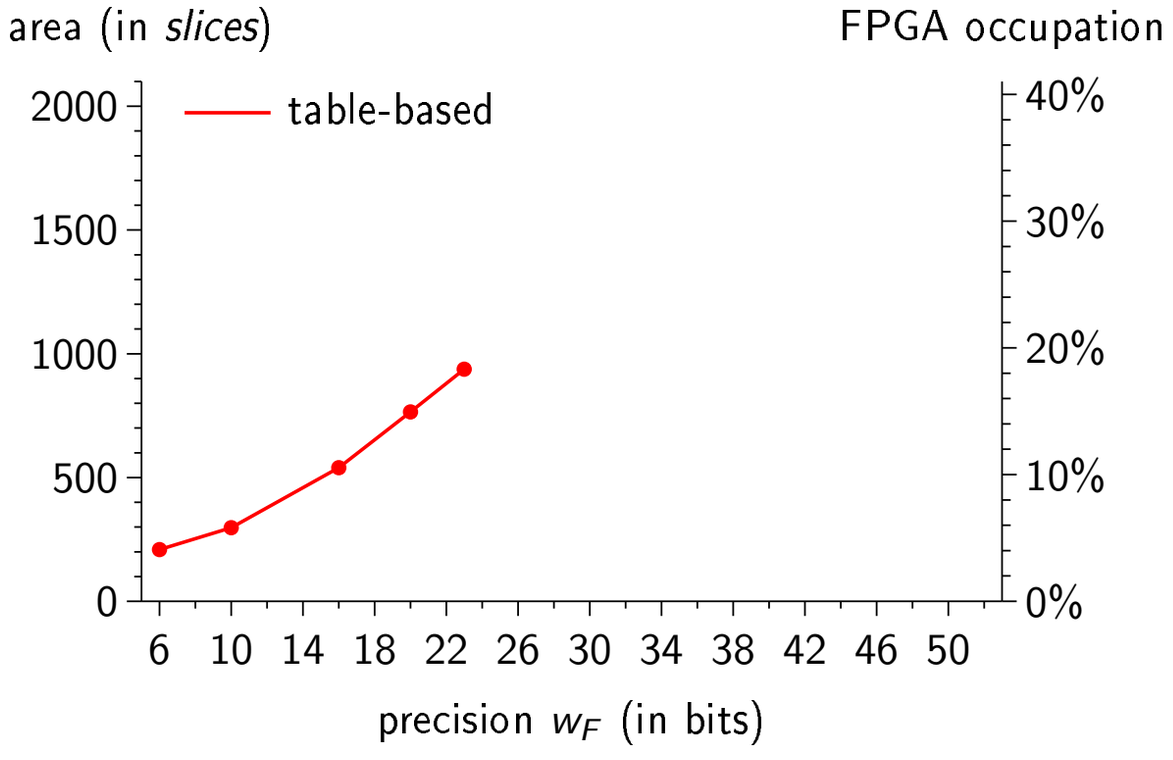

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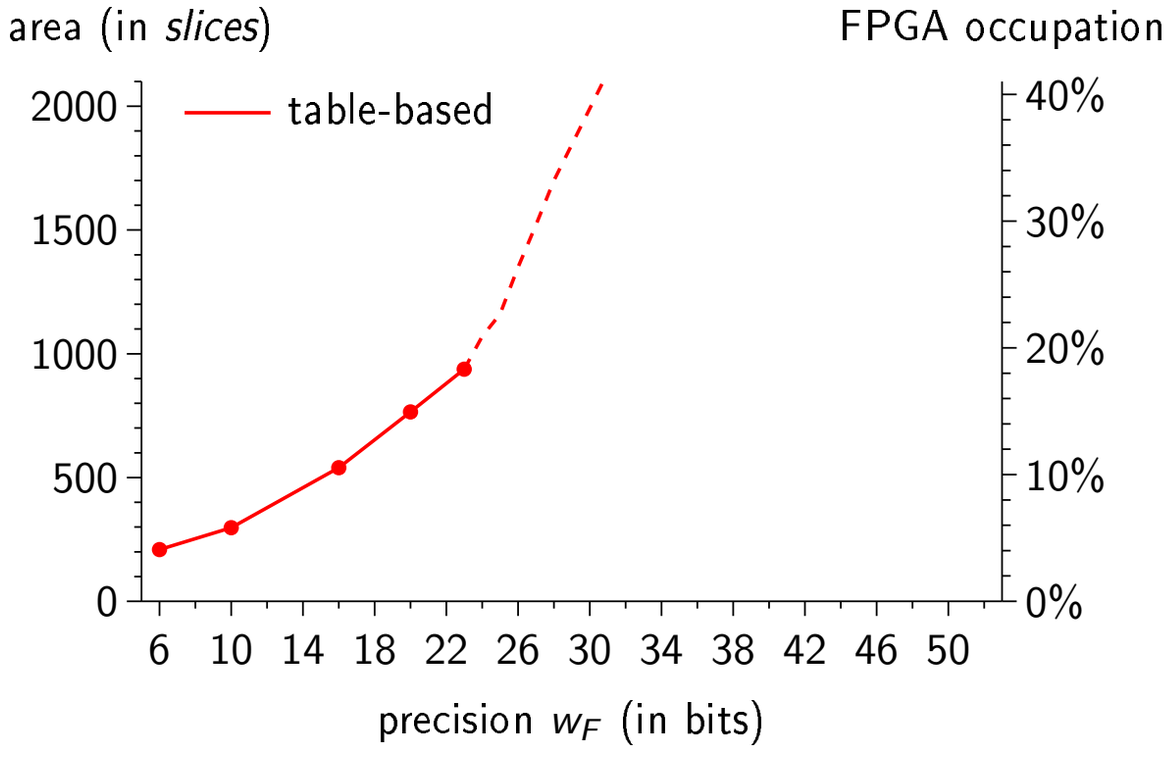

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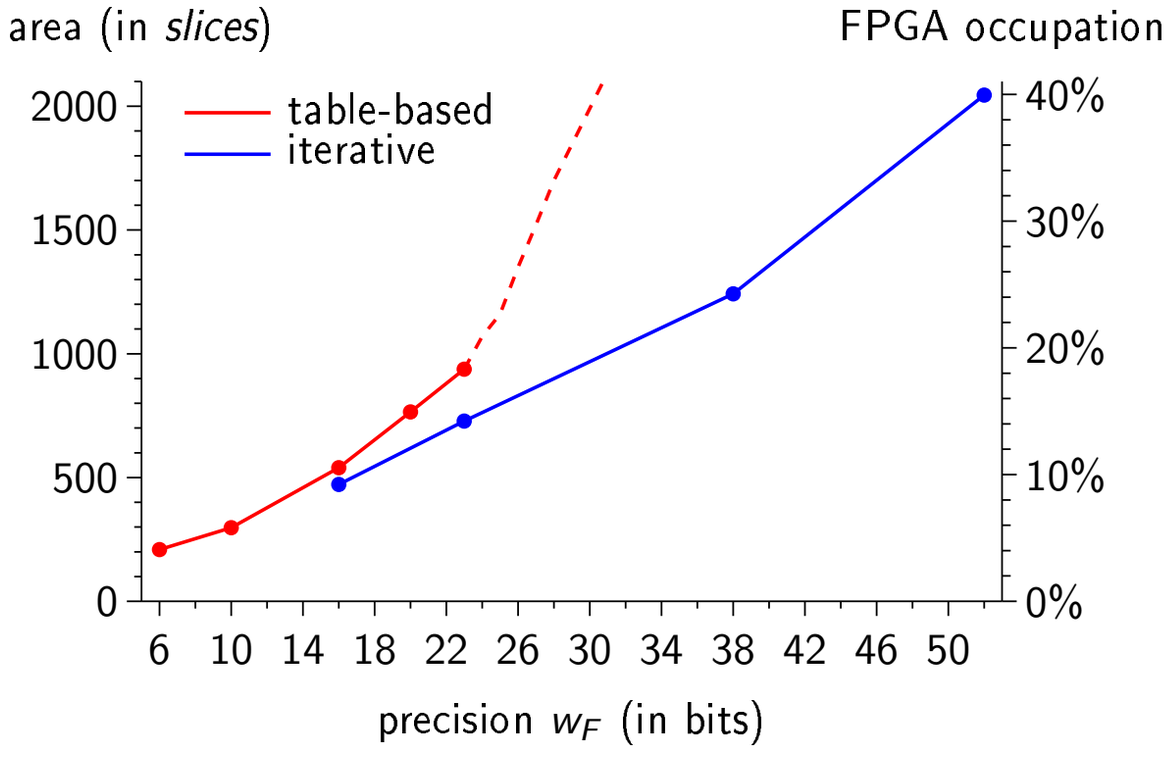

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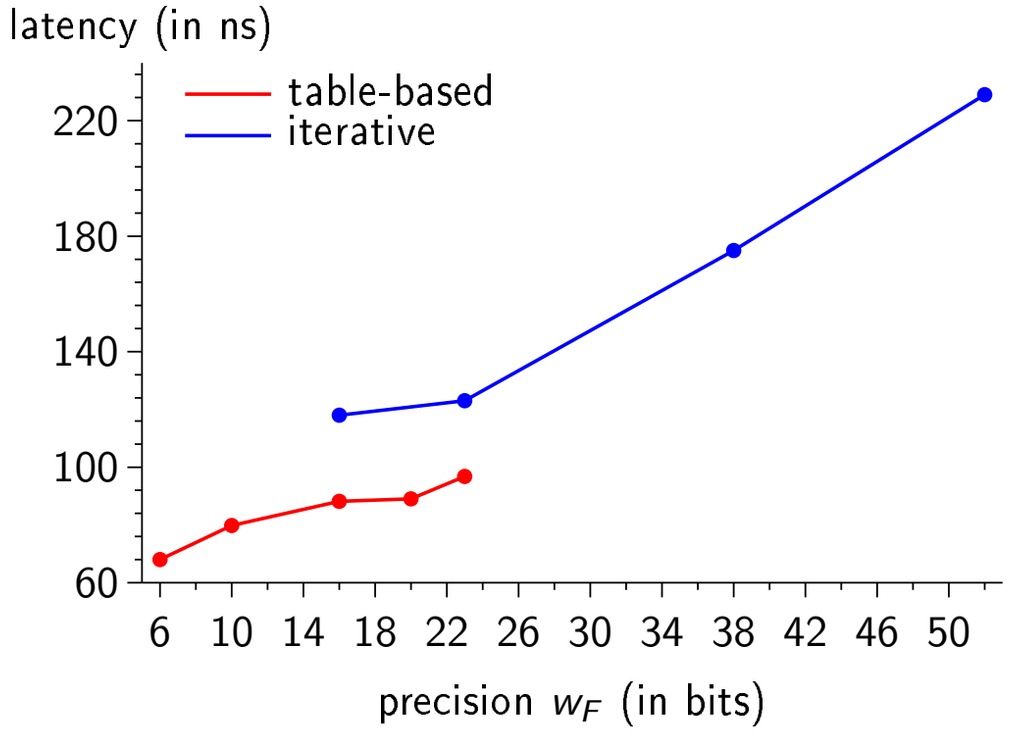
- double precision $(w_E, w_F) = (11, 52)$ (iterative method): 2045 slices (40%)

Operator latency (exponential)



- single precision $(w_E, w_F) = (8, 23)$ (table-based method): 97 ns
- double precision $(w_E, w_F) = (11, 52)$ (iterative method): 229 ns

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Our contribution

- exponential and logarithm operators
- up to double precision
- guaranteed faithful rounding
- scalable method
- hardware-specific algorithms: fast and cheap operators

Future work

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- implement double precision for other functions for FPLibrary
- study compound functions

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- implement double precision for other functions for FPLibrary
- study compound functions
- careful error analysis:
  - certified algorithms and operators
  - generic proofs (Gappa)
- most of this work is not FPGA-specific: extend it to ASICs

Thank you for your attention

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Questions?